

STUDENT HAND BOOK 2024-25

(3-2)

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Vision of the Institute

To be recognized as a premier institution in offering the value based and futuristic quality technical education to meet the technological need of the society.

Mission of the the Institute

- To impart value quality technical education through innovative teaching and learning methods.
- To continuously produce employable technical graduates with advanced technical skills to meet the current and future technological need of the society.
- To prepare the graduate for high learning with emphasis on academic and industrial research.

Vision of the Department

To promote excellence in technical education and scientific research in electronics and communication engineering for the benefit of society.

Mission of the Department:

- To impart excellent technical education with state of art facilities inculcating values and lifelong learning attitude.
- To develop core competence in our students imbibing professional ethics and team spirit.
- To encourage research benefiting society through higher learning

PEOs:

PEO 1: Establish themselves as successful professionals in their career and higher education in the field of Electronics & Communication Engineering and allied domains through rigorous quality education.

PEO 2: Develop Professionalism, Ethical values, Excellent Leadership qualities, Communication Skills and teamwork in their Professional front and adapt to current trends by engaging in lifelong learning

PEO 3: Apply the acquired knowledge & skills to develop novel technology and products for solving real life problems those are economically feasible and socially relevant

PEO 4: To prepare the graduates for developing administrative acumen, to adapt diversified and multidisciplinary platforms to compete globally.

Quality Policy:

Our quality policy is to continuously strive for over-all development of the department and the students. Our policy is to provide best inputs to the students and to develop them to imbibe the spirit of professionalism, dedication & commitment.

Dress Code

We encourage our students to be formally dressed on and off campus. This nurtures the feeling of equality and belongings among the students fraternity.

All students are required to carry Photo Identity card at all the time while in the campus

POs:

PO1: Engineering Knowledge: Apply knowledge of mathematics, natural science, computing, engineering fundamentals and an engineering specialization as specified in WK1 to WK4 respectively to develop to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions with consideration for sustainable development. (WK1 to WK4)

PO3: Design/Development of Solutions: Design creative solutions for complex engineering problems and design/develop systems/components/processes to meet identified needs with consideration for the public health and safety, whole-life cost, net zero carbon, culture, society and environment as required. (WK5)

PO4: Conduct Investigations of Complex Problems: Conduct investigations of complex engineering problems using research-based knowledge including design of experiments, modelling, analysis & interpretation of data to provide valid conclusions. (WK8).

PO5: Engineering Tool Usage: Create, select and apply appropriate techniques, resources and modern engineering & IT tools, including prediction and modelling recognizing their limitations to solve complex engineering problems. (WK2 and WK6)

PO6: The Engineer and The World: Analyze and evaluate societal and environmental aspects while solving complex engineering problems for its impact on sustainability with reference to economy, health, safety, legal framework, culture and environment. (WK1, WK5, and WK7).

PO7: Ethics: Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national & international laws. (WK9)

PO8: Individual and Collaborative Team work: Function effectively as an individual, and as a member or leader in diverse/multi-disciplinary teams.

PO9: Communication: Communicate effectively and inclusively within the engineering community and society at large, such as being able to comprehend and write effective reports and design documentation, make

effective presentations considering cultural, language, and learning differences

PO10: Project Management and Finance: Apply knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.

PO11: Life-Long Learning: Recognize the need for, and have the preparation and ability for

i) independent and life-long learning ii) adaptability to new and emerging technologies and iii) critical thinking in the broadest context of technological change. (WK8)

PSOs:

- Ability to apply concepts of Electronics & Communication Engineering to associated research areas of electronics, communication, signal processing, VLSI, Embedded systems
- Ability to design, analyze and simulate a variety of Electronics & Communication functional elements using hardware and software tools along with analytic skill

A Bird's Eye view about the Institution

CMR Engineering College, popularly known as CMREC is the brain child of the clairvoyant CH.Narasihma Reddy. CMR Engineering College is one of the best engineering Colleges for aspiring engineering students. It is one of the newly established Colleges by CMR Engineering Educational Society. CMR Engineering College was established in 2010 in 10 Acres and built up area of 4,785.78 Sq.m. with a single - minded aim to provide a perfect platform to students in the field of Engineering, Technology for their academic and overall personality development. The college has a very good academic activity which focuses for the campus placement.

The college is approved by the All India Council for Technical Education, New Delhi and is affiliated to JNT University Hyderabad. The CMREC is offering the three under graduate courses in ECE, CSE and MECH, and post graduate course in ECE and CSE.

Today, CMREC has grown in leaps and bounds and it is no wonder that CMREC has become cynosure of the eyes of many, hankering for the distinguished centre of technological learning.

Discipline, Character and Education are the three tenets for which CMREC stands, is certainly the haven where values blend seamlessly to churn out engineers for future.

- Collaborating with Institutions and Industries.
- Promoting research and development programme for the growth of economy.
- Disseminating technical knowledge in the region by continuing education programmes.
- Aiming at continual improvement of all round development of student

Department Profile

The Department of Electronics and Communication engineering of CMR Engineering College was established in the academic year 2010-11 with an annual intake of 120. The intake was increased to 180 from the academic year 2012-13 and later the intake was increased to 240 from the academic year 2013-14. In addition to this intake, the Department has 20% lateral entry students at II B.Tech level.

M.Tech programme was started with 24 intake in the specialization of Embedded Systems from the year 2013-14 and VLSI System Design from the year 2014-15.

The B.Tech (ECE) program is duly approved by the AICTE and Government of Telangana and affiliated to Jawaharlal Nehru Technological University (JNTUH), Hyderabad. Three batches have graduated so far.

Department have 56 faculty and are members of professional bodies like ISTE, IEEE, IETE. Some of the students are the members of IETE student forum and IEEE student branch of the existing

Department. A technical association (ECMRON) of ECE has been formed by the senior students of the department for the benefits of students to impart additional knowledge in the field of E&C Engineering apart from prescribed curriculum.

The Department has well equipped state of art laboratories to gain good knowledge and technical skills in the field of Electronics, Communication, Microwave, VLSI, Digital Signal Processing & Microprocessors & Microcontrollers. The Department periodically organizes seminars, symposia, workshops and guest lectures for the benefit of both the students and the faculty.

**Academic Regulations, Course Structure
and Detailed Syllabus under Autonomous
Status**

BACHELOR OF TECHNOLOGY (B.TECH.)

(CMREC - R-22 Regulations)

(Applicable for the batch admitted from 2022-2023)

PRELIMINARY DEFINITIONS AND NOMENCLATURES

AICTE: Means All India Council for Technical Education, New Delhi.

Autonomous Institute: Means an institute designated as Autonomous by University Grants Commission (UGC), New Delhi in concurrence with affiliating University (Jawaharlal Nehru Technological University, Hyderabad) and State Government of Telangana.

Academic Autonomy: Means freedom to an institute in all aspects of conducting its academic programs, granted by UGC for Promoting Excellence.

Academic Council: The Academic Council is the highest academic body of the institute and is responsible for the maintenance of standards of instruction, education and examination within the institute. Academic Council is an authority as per UGC regulations and it has the right to take decisions on all academic matters including academic research.

Academic Year: It is the period necessary to complete an actual course of study within a year. It comprises two main semesters i.e., (one odd + one even) and supplementary semester.

Branch: Means specialization in a program like B.Tech. Degree program in Electronics and communication Engineering, B.Tech degree program in Computer Science and Engineering, etc.

Board of Studies (BOS): BOS is an authority as defined in UGC regulations, constituted by Head of the Organization for each of the departments separately. They are responsible for curriculum design and updation in respect of all the programs offered by a department.

Backlog Course: A course is considered to be a backlog course, if the student has obtained a failure grade (F) in that course.

Basic Sciences: The courses offered in the areas of Mathematics, Physics, Chemistry etc., are considered to be foundational in nature.

Commission: Means University Grants Commission (UGC), New Delhi.

Choice Based Credit System: The credit based semester system is one which provides flexibility in designing curriculum and assigning credits based on the course content and hours of teaching along with provision of choice for the student in the course selection.

Compulsory course: Course required to be undertaken for the award of the degree as per the program.

Continuous Internal Examination: It is an examination conducted towards sessional assessment.

Core: The courses that are essential constituents of each engineering discipline are categorized as professional core courses for that discipline.

Course: A course is a subject offered by a department for learning in a particular semester.

Course Outcomes: The essential skills that need to be acquired by every student through a course.

Credit: A credit is a unit that gives weight to the value, level or time requirements of an academic course. The number of 'Contact Hours' in a week of a particular course determines its credit value. One credit is equivalent to one lecture/tutorial/lab hour per week.

Credit point: It is the product of grade point and number of credits for a course.

Cumulative Grade Point Average (CGPA): It is a measure of cumulative performance of a student over all the completed semesters. The CGPA is the ratio of total credit points secured by a student in various courses in all semesters and the sum of the total credits of all courses in all the semesters. It is expressed up to two decimal places.

Curriculum: Curriculum incorporates the planned interaction of students with instructional content, materials, resources, and processes for evaluating the attainment of Program Educational Objectives.

Department: An academic entity that conducts relevant curricular and co-curricular activities, involving both teaching and non-teaching staff, and other resources in the process of study for a degree.

Dropping from Semester: Student who does not want to register for any semester can apply in writing in prescribed format before the commencement of that semester.

Elective Course: A course that can be chosen from a set of courses. An elective can be Professional Elective and or Open Elective.

Evaluation: Evaluation is the process of judging the academic performance of the student in her/his courses. It is done through a combination of continuous internal assessment and semester end examinations.

Grade: It is an index of the performance of the students in a said course. Grades are indicated by alphabets.

Grade Point: It is a numerical weight allotted to each letter grade on a 10 - point scale.

Honors: An Honors degree typically refers to a higher level of academic achievement at an undergraduate level.

Institute: Means CMR Engineering, Hyderabad unless indicated otherwise by the context.

Massive Open Online Courses (MOOC): MOOC courses inculcate the habit of self-learning. MOOC courses would be additional choices in all the elective group courses.

Minor: Minor are coherent sequences of courses which may be taken in addition to the courses required for the B.Tech. Degree.

Pre-requisite: A specific course or subject, the knowledge of which is required to complete before student register another course at the next grade level.

Professional Elective: It indicates a course that is discipline centric. An appropriate choice of minimum number of such electives as specified in the program will lead to a degree with specialization.

Program: Means, UG degree program: Bachelor of Technology (B.Tech.) and PG degree program: Master of Technology (M.Tech.).

Program Educational Objectives: The broad career, professional and personal goals that every student will achieve through a strategic and sequential action plan.

Project work: It is a design or research based work to be taken up by a student during his/her final year to achieve a particular aim. It is a credit based course and is to be planned carefully by the student.

Re-Appearing: A student can reappear only in the semester end examination for theory component of a course, subject to the regulations contained herein.

Registration: Process of enrolling into a set of courses in a semester of a program.

Regulations: The regulations, common to all B.Tech. Programs offered by Institute, are designated as – CMREC Regulations – R-22 and are binding on all the stakeholders.

Semester: It is a period of study consisting of 15 to 18 weeks of academic work equivalent to normally 90 working days. Odd semester commences usually in July and even semester in December of every year.

Semester End Examinations: It is an examination conducted for all courses offered in a semester at the end of the semester.

Student Outcomes: The essential skill sets that need to be acquired by every student during her/his program of study. These skill sets are in the areas of employability, entrepreneurial, social and behavioral.

University: Means Jawaharlal Nehru Technological University Hyderabad (JNTUH), Hyderabad, is an affiliating University.

Withdraw from a Course: Withdrawing from a course means that a student can drop from a course within the first two weeks of odd or even semester. However, he / she can choose a substitute course in place of it by exercising the option within 5 working days from the date of withdrawal.

FOREWORD

The autonomy is conferred to **CMR Engineering College (CMREC)**, Hyderabad by University Grants Commission (UGC), New Delhi based on its performance as well as future commitment and competency to impart quality education. It is a mark of its ability to function independently in accordance with the set norms of the monitoring bodies including JNT University Hyderabad (JNTUH), Hyderabad and AICTE, New Delhi. It reflects the confidence of the affiliating University in the autonomous institution to uphold and maintain standards it expects to deliver on its own behalf. Thus, an autonomous institution is given the freedom to have its own **examination system** and **monitoring mechanism**, independent of the affiliating University but under its observance.

CMREC is proud to win the credence of all the above bodies monitoring the quality in education and has gladly accepted the responsibility of sustaining, if not improving upon the standards and ethics for which it has been striving for more than a decade in reaching its present standing in the arena of contemporary technical education. As a follow up, statutory bodies such as Academic Council and Board of Studies (BOS) are constituted with the guidance of the Governing Body of the institute and recommendations of the JNTUH to frame the regulations, course structure, and syllabi under autonomous status.

The autonomous regulations, course structure, and syllabi have been prepared after prolonged and detailed interaction with several expertise solicited from academics, industry and research, in accordance with the vision and mission of the institute in order to produce a quality engineering graduate to the society.

All the faculty, parents, and students are requested to go through all the rules and regulations carefully. Any clarifications needed are to be sought at appropriate time and from the principal of the institute, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The cooperation of all the stake holders is requested for the successful implementation of the autonomous system in the larger interests of the institute and brighter prospects of engineering graduates.

PRINCIPAL

ACADEMIC REGULATIONS (R22) FOR B.TECH REGULAR

STUDENTS WITH EFFECT FROM THE ACADEMIC YEAR

2022-23

1.0 Under-Graduate Degree Programme in Engineering & Technology (UGP in E&T)

Jawaharlal Nehru Technological University Hyderabad (JNTUH) offers a 4-year (8 semesters) **Bachelor of Technology** (B.Tech.) degree programme, under Choice Based Credit System (CBCS) at its non-autonomous constituent and affiliated colleges with effect from the academic year **2022-23**.

Eligibility for Admission

Admission to the undergraduate (UG) programme shall be made either on the basis of the merit rank obtained by the qualified student in entrance test conducted by the Telangana State Government (EAMCET) or the University or on the basis of any other order of merit approved by the University, subject to reservations as prescribed by the government from time to time.

The medium of instructions for the entire undergraduate programme in Engineering & Technology will be **English** only.

B.Tech. Programme Structure

A student after securing admission shall complete the B.Tech. programme in a minimum period of **four** academic years (8 semesters), and a maximum period of **eight** academic years (16 semesters) starting from the date of commencement of first year first semester, failing which student shall forfeit seat in B.Tech course. Each student shall secure 160 credits (with CGPA ≥ 5) required for the completion of the undergraduate programme and award of the B.Tech. Degree.

UGC/ AICTE specified definitions/ descriptions are adopted appropriately for various terms and abbreviations used in these academic regulations/ norms, which are listed below.

Semester Scheme

Each undergraduate programme is of 4 academic years (8 semesters) with the academic year divided into two semesters of 22 weeks (≥ 90 instructional days) each and in each

semester - „Continuous Internal Evaluation (CIE)“ and „Semester End Examination (SEE)“ under Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) indicated by UGC, and curriculum/course structure suggested by AICTE are followed.

Credit Courses

All subjects/ courses are to be registered by the student in a semester to earn credits which shall be assigned to each subject/ course in an L: T: P: C (lecture periods: tutorial periods: practical periods: credits) structure based on the following general pattern.

- One credit for one hour/ week/ semester for Theory/ Lecture (L) courses or Tutorials.
- One credit for two hours/ week/ semester for Laboratory/ Practical (P) courses.

Courses like Environmental Science, Constitution of India, Intellectual Property Rights, and Gender Sensitization Lab are mandatory courses. These courses will not carry any credits.

Subject Course Classification

All subjects/ courses offered for the undergraduate programme in E&T (B.Tech. degree programmes) are broadly classified as follows. The University has followed almost all the guidelines issued by AICTE/UGC.

S. No.	Broad Course Classification	Course Group/ Category	Course Description
1	Foundation Courses (FnC)	BS – Basic Sciences	Includes Mathematics, Physics and Chemistry subjects
2		ES - Engineering Sciences	Includes Fundamental Engineering Subjects
3		HS – Humanities and Social Sciences	Includes subjects related to Humanities, Social Sciences and Management
4	Core Courses (CoC)	PC – Professional Core	Includes core subjects related to the parent discipline/ department/ branch of Engineering.
5	Elective Courses (ElC)	PE – Professional Electives	Includes elective subjects related to the parent discipline/ department/ branch of Engineering.
6		OE – Open Electives	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline/ department/ branch of Engineering.
7	Core Courses	Project Work	B.Tech. Project or UG Project or UG Major Project or Project Stage I & II
8		Industry Training/ Internship/ Industry Oriented Mini-project/ Mini-Project/ Skill Development Courses	Industry Training/ Internship/ Industry Oriented Mini-Project/ Mini-Project/ Skill Development Courses
9		project/ Mini-Project/ Skill Development Courses	
		Seminar	Seminar/ Colloquium based on core contents related to parent discipline/ department/ branch of Engineering.
10	Minor Courses	-	1 or 2 Credit Courses (subset of HS)
11	Mandatory Courses (MC)	-	Mandatory Courses (non-credit)

Course Registration

A „faculty advisor or counselor“ shall be assigned to a group of 20 students, who will advise the students about the undergraduate programme, its course structure and curriculum, choice/option for subjects/ courses, based on their competence, progress, pre-requisites and interest.

The academic section of the college invites „registration forms“ from students before the beginning of the semester through „on-line registration“, ensuring „date and time stamping“. The online registration requests for any „current semester“ shall be **completed before the commencement of SEEs (Semester End Examinations) of the ‘preceding semester’**.

A student can apply for **on-line** registration, **only after** obtaining the „**written approval**“ from faculty advisor/counselor, which should be submitted to the college academic section through the Head of the Department. A copy of it shall be retained with the Head of the Department, Faculty Advisor/ Counselor and the student.

A student may be permitted to register for all the subjects/ courses in a semester as specified in the course structure with maximum additional subject(s)/course(s) limited to 6 Credits (any 2 elective subjects), based on **progress** and SGPA/ CGPA, and completion of the „**pre-requisites**“ as indicated for various subjects/ courses, in the department course structure and syllabus contents.

Choice for „**additional subjects/courses**“, not more than any 2 elective subjects in any Semester, must be clearly indicated, which needs the specific approval and signature of the Faculty Advisor/Mentor/HOD.

If the student submits ambiguous choices or multiple options or erroneous entries during **online** registration for the subject(s) / course(s) under a given/ specified course group/ category as listed in the course structure, only the first mentioned subject/ course in that category will be taken into consideration.

Subject/ course options exercised through **on-line** registration are final and **cannot** be changed or inter-changed; further, alternate choices also will not be considered. However, if the subject/ course that has already been listed for registration by the Head of the Department in a semester could not be offered due to any inevitable or unexpected reasons, then the student shall be allowed to have alternate choice either for

a new subject (subject to offering of such a subject), or for another existing subject (subject to availability of seats). Such alternate arrangements will be made by the Head of the Department, with due notification and time-framed schedule, within a **week** after the commencement of class-work for that semester.

Dropping of subjects/ courses may be permitted, only after obtaining prior approval from the faculty advisor/ counselor „within a period of 15 days“ from the beginning of the current semester.

Open Electives: The students have to choose three Open Electives (OE-I, II & III) from the list of Open Electives given by other departments. However, the student can

opt for an Open Elective subject offered by his own (parent) department, if the student has not registered and not studied that subject under any category (Professional Core,

Professional Electives, Mandatory Courses etc.) offered by parent department in any semester. Open Elective subjects already studied should not repeat/should not match with any category (Professional Core, Professional Electives, Mandatory Courses etc.) of subjects even in the forthcoming semesters.

Professional Electives: The students have to choose six Professional Electives (PE-I to VI) from the list of professional electives given.

Subjects/ courses to be offered

A subject/ course may be offered to the students, **only if** a minimum of 15 students opt for it.

More than **one faculty member** may offer the **same subject** (lab/ practical may be included with the corresponding theory subject in the same semester) in any semester. However, selection of choice for students will be based on - „**first come first serve** basis and CGPA criterion“ (i.e. the first focus shall be on early **on-line entry** from the student for registration in that semester, and the second focus, if needed, will be on CGPA of the student).

If more entries for registration of a subject come into picture, then the Head of the Department concerned shall decide, whether or not to offer such a subject/ course for **two (or multiple) sections**.

In case of options coming from students of other departments/ branches/ disciplines (not considering **open electives**), first **priority** shall be given to the student of the „**parent department**“.

Attendance requirements:

A student shall be eligible to appear for the semester end examinations, if the student acquires a minimum of 75% of attendance in aggregate of all the subjects/ courses (including attendance in mandatory courses like Environmental Science, Constitution of India, Intellectual Property Rights, and Gender Sensitization Lab) for that semester. **Two periods** of attendance for each theory subject shall be considered, if the student appears for the mid-term examination of that subject. **This attendance should also be Included in the attendance uploaded every fortnight in the University Website.**

Shortage of attendance in aggregate up to 10% (65% and above, and below 75%) in each semester may be condoned by the college academic committee on genuine and valid grounds, based on the student's representation with supporting evidence.

A stipulated fee shall be payable for condoning of shortage of attendance.

Shortage of attendance below 65% in aggregate shall in **NO** case be condoned.

Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examinations of that semester. They get detained and their registration for that semester shall stand cancelled, including all academic credentials (internal marks etc.) of that semester. They will not be promoted to the

next semester. They may seek re-registration for all those subjects registered in that semester in which the student is detained, by seeking re-admission into that semester as

and when offered; if there are any professional electives and/ or open electives, the same may also be re-registered if offered. However, if those electives are not offered in later semesters, then alternate electives may be chosen from the **same** set of elective subjects offered under that category.

A student fulfilling the attendance requirement in the present semester shall not be eligible for readmission into the same class.

Academic Requirements

The following academic requirements have to be satisfied, in addition to the attendance requirements mentioned in Item No. 6.

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course, if student secures not less than 35% (14 marks out of 40 marks) in the Continuous Internal Evaluation (CIE), not less than 35% (21 marks out of 60 marks) in the semester end examinations (SEE), and a minimum of 40% (40 marks out of 100 marks) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together; in terms of letter grades, this implies securing 'C' grade or above in that subject/ course.

A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to Real-time Research Project (or) Field Based Research Project (or) Industry Oriented Mini Project (or) Internship (or) Seminar, if the student secures not less than 40% marks (i.e. 40 out of 100 allotted marks) in each of them. The student is deemed to have failed, if he (i) does not submit a report on Industry Oriented Mini Project/Internship, or (ii) not make a presentation of the same before the evaluation committee as per schedule, or (iii) secures less than 40% marks in Real-time Research Project (or) Field Based Research Project (or) Industry Oriented Mini Project (or) Internship evaluations.

A student may reappear once for each of the above evaluations, when they are scheduled again; if the student fails in such „one reappearance“ evaluation also, the student has to reappear for the same in the next subsequent semester, as and when it is scheduled.

Promotion Rules:

S. No.	Promotion	Conditions to be fulfilled
1	First year first semester to first year second semester	Regular course of study of first year first semester.
2	First year second semester to Second year first semester	(i) Regular course of study of first year second semester. (ii) Must have secured at least 20 credits out of 40 credits i.e., 50% credits up to first year second semester from all the relevant regular and supplementary examinations, whether the student takes those examinations or not.
3.	Second year first semester to Second year second semester	Regular course of study of second year first semester.
4	Second year second semester to Third year first semester	(i) Regular course of study of second year second semester. (ii) Must have secured at least 48 credits out of 80 credits i.e., 60% credits up to second year second semester from all the relevant regular and supplementary examinations, whether the student takes those examinations or not.
5	Third year first semester to Third year second semester	Regular course of study of third year first semester.
6	Third year second semester to Fourth year first semester	(i) Regular course of study of third year second semester. (ii) Must have secured at least 72 credits out of 120 credits i.e., 60% credits up to third year second semester from all the relevant regular and supplementary examinations, whether the student takes those examinations or not.
7	Fourth year first semester to Fourth year second semester	Regular course of study of fourth year first semester.

A student (i) shall register for all courses/subjects covering 160 credits as specified and listed in the course structure, (ii) fulfills all the attendance and academic requirements for 160 credits, (iii) earn all 160 credits by securing $SGPA \geq 5.0$ (in each semester), and $CGPA \geq 5$ (at the end of 8 semesters), (iv) **passes all the mandatory courses**, to successfully complete the undergraduate programme. The performance of the student in these 160 credits shall be considered for the calculation of the final CGPA (**at the end of undergraduate programme**), and shall be indicated in the grade card / marks memo of IV-year II semester.

If a student registers for „**extra subjects**’ (in the parent department or other departments/branches of Engg.) other than those listed subjects totaling to 160 credits as specified in the course structure of his department, the performances in those „**extra subjects**” (although evaluated and graded using the same procedure as that of the required 160 credits) will not be considered while calculating the SGPA and CGPA. For such „**extra subjects**’ registered, percentage of marks and letter grade alone will be indicated in the grade card / marks memo as a performance measure, subject to completion of the attendance and academic requirements as stated in regulations Items 6 and 7.1 – 7.4 above.

A student eligible to appear in the semester end examination for any subject/ course, but absent from it or failed (thereby failing to secure ‘C’ grade or above) may reappear for that subject/ course in the supplementary examination as and when conducted. In such cases, internal marks (CIE) assessed earlier for that subject/ course will be carried over, and added to the marks to be obtained in the SEE supplementary examination for evaluating performance in that subject.

A student **detained in a semester due to shortage of attendance may be re-admitted in the same semester in the next academic year for fulfillment of academic requirements**. The academic regulations under which a student has been re-admitted shall be applicable. Further, no grade allotments or SGPA/ CGPA calculations will be done for the entire semester in which the student has been detained.

A student **detained due to lack of credits, shall be promoted to the next academic year only after acquiring the required number of academic credits**. The academic regulations under which the student has been readmitted shall be applicable to him.

Evaluation - Distribution and Weightage of Marks

The performance of a student in every subject/course (including practical’s and Project Stage – I & II) will be evaluated for 100 marks each, with 40 marks allotted for CIE (Continuous Internal Evaluation) and 60 marks for SEE (Semester End-Examination).

In CIE, for theory subjects, during a semester, there shall be two mid-term examinations. Each Mid-Term examination consists of two parts i) **Part – A** for 10 marks, ii) **Part – B** for 20 marks with a total duration of 2 hours as follows:

1. Mid Term Examination for 30 marks:
 - a. Part - A : Objective/quiz paper/Short Answers for 10 marks.(5*2=10Marks)

b. Part - B : Descriptive paper for 20 marks.

The objective/quiz paper is set with multiple choice, fill-in the blanks and match the following type of questions for a total of 10 marks. The descriptive paper shall contain 6 full questions out of which, the student has to answer 4 questions, each carrying 5 marks. The **average of the two Mid Term Examinations** shall be taken as the final marks for Mid Term Examination (for 30 marks).

The remaining 10 marks of Continuous Internal Evaluation are distributed as:

2. Assignment for 5 marks. (**Average of 2 Assignments** each for 5 marks)
3. Subject Viva-Voce/PPT/Poster Presentation/ Case Study on a topic in the concerned subject for 5 marks.

While the first mid-term examination shall be conducted on 50% of the syllabus, the second mid-term examination shall be conducted on the remaining 50% of the syllabus.

Five (5) marks are allocated for assignments (as specified by the subject teacher concerned). The first assignment should be submitted before the conduct of the first mid-term examination, and the second assignment should be submitted before the conduct of the second mid-term examination. The average of the two assignments shall be taken as the final marks for assignment (for 5 marks).

Subject Viva-Voce/PPT/Poster Presentation/ Case Study on a topic in the subject concerned for 5 marks before II Mid-Term Examination.

- The Student, in each subject, shall have to earn 35% of marks (i.e. 14 marks out of 40 marks) in CIE, 35% of marks (i.e. 21 marks out of 60) in SEE and Overall 40% of marks (i.e. 40 marks out of 100 marks) both CIE and SEE marks put together.

The student is eligible to write Semester End Examination of the concerned subject, if the student scores $\geq 35\%$ (14 marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned subject but not scored minimum 35% of CIE marks (14 marks out of 40 internal marks), his performance in that subject in SEE shall stand cancelled inspite of appearing the SEE.

There is NO Computer Based Test (CBT) for R22 regulations. The

details of the end semester question paper pattern are as follows:

The semester end examinations (SEE), for theory subjects, will be conducted for 60 marks consisting of two parts viz. i) **Part- A** for 10 marks, ii) **Part - B** for 50 marks.

- Part-A is a compulsory question which consists of ten sub-questions from all units carrying equal marks.
- Part-B consists of five questions (numbered from 2 to 6) carrying 10 marks each.

Each of these questions is from each unit and may contain sub-questions. For each

question there will be an “either” “or” choice, which means that there will be two questions from each unit and the student should answer either of the two questions.

- The duration of Semester End Examination is 3 hours.

For practical subjects there shall be a Continuous Internal Evaluation (CIE) during the semester for 40 marks and 60 marks for semester end examination. Out of the 40 marks for internal evaluation:

1. A write-up on day-to-day experiment in the laboratory (in terms of aim, components/procedure, expected outcome) which shall be evaluated for 10 marks
2. **10 marks for viva-voce** (or) tutorial (or) case study (or) application (or) poster presentation of the course concerned.
3. Internal practical examination conducted by the laboratory teacher concerned shall be evaluated for 10 marks.
4. The remaining 10 marks are for Laboratory Project, which consists of the Design (or) Software / Hardware Model Presentation (or) App Development (or) Prototype Presentation submission which shall be evaluated after completion of laboratory course and before semester end practical examination.

The Semester End Examination shall be conducted with an external examiner and the laboratory teacher. The external examiner shall be appointed from the cluster / other colleges which will be decided by the examination branch of the University.

In the Semester End Examination held for 3 hours, total 60 marks are divided and allocated as shown below:

1. 10 marks for write-up
 2. 15 for experiment/program
 3. 15 for evaluation of results
 4. 10 marks for presentation on another experiment/program in the same laboratory course and
 5. 10 marks for viva-voce on concerned laboratory course.
- The Student, in each subject, shall have to earn 35% of marks (i.e. 14 marks out of 40 marks) in CIE, 35% of marks (i.e. 21 marks out of 60) in SEE and Overall 40% of marks (i.e. 40 marks out of 100 marks) both CIE and SEE marks put together.

The student is eligible to write Semester End Examination of the concerned subject, if the student scores $\geq 35\%$ (14 marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned subject but not scored minimum 35% of CIE marks (14 marks out of 40 internal marks), his performance in that subject in SEE shall stand cancelled inspite of appearing the SEE.

There shall be an Industry training (or) Internship (or) Industry oriented Mini-project (or) Skill Development Courses (or) Paper presentation in reputed journal (or) Industry Oriented Mini Project in collaboration with an industry of their specialization. Students shall register for this immediately after II-Year II Semester Examinations and pursue it during summer vacation/semester break & during III Year without effecting regular course work. Internship at reputed organization (or) Skill development courses (or) Paper presentation in reputed journal (or) Industry Oriented Mini Project shall be submitted in a report form and presented before the committee in III-year II semester before end semester examination. It shall be evaluated for 100 external marks. The committee consists of an External Examiner, Head of the Department, Supervisor of the Industry Oriented Mini Project (or) Internship etc, Internal Supervisor and a Senior Faculty Member of the Department. There shall be **NO internal marks** for Industry Training (or) Internship (or) Mini-Project (or) Skill Development Courses (or) Paper Presentation in reputed journal (or) Industry Oriented Mini Project.

The UG project shall be initiated at the end of the IV Year I Semester and the duration of the project work is one semester. The student must present Project Stage – I during IV Year I Semester before II Mid examinations, in consultation with his Supervisor, the title, objective and plan of action of his Project work to the departmental committee for approval before commencement of IV Year II Semester. Only after obtaining the approval of the departmental committee, the student can start his project work.

UG project work shall be carried out in two stages: Project Stage – I for approval of project before Mid-II examinations in IV Year I Semester and Project Stage – II during IV Year II Semester. Student has to submit project work report at the end of IV Year II Semester. The project shall be evaluated for 100 marks before commencement of SEE Theory examinations.

For Project Stage – I, the departmental committee consisting of Head of the Department, project supervisor and a senior faculty member shall approve the project work to begin before II Mid-Term examination of IV Year I Semester. The student is deemed to be not eligible to register for the Project work, if he does not submit a report on Project Stage - I or does not make a presentation of the same before the evaluation committee as per schedule.

A student who has failed may reappear once for the above evaluation, when it is scheduled again; if he fails in such „one reappearance“ evaluation also, he has to reappear for the same in the next subsequent semester, as and when it is scheduled.

For Project Stage – II, the external examiner shall evaluate the project work for 60 marks and the internal project committee shall evaluate it for 40 marks. Out of 40 internal marks, the departmental committee consisting of Head of the Department, Project Supervisor and a Senior Faculty Member shall evaluate the project work for 20 marks and Project Supervisor shall evaluate for 20 marks. The topics for Industry Oriented Mini Project/ Internship/SDC etc. and the main Project shall be different from the topic already taken. The student is deemed to have failed, if he (i) does not submit a

report on the Project, or (ii) does not make a presentation of the same before the External Examiner as per schedule, or (iii) secures less than 40% marks in the sum total of the CIE and SEE taken together.

For conducting viva-voce of project, University selects an external examiner from the list of experts in the relevant branch submitted by the Principal of the College.

A student who has failed, may reappear once for the above evaluation, when it is scheduled again; if student fails in such „one reappearance“ evaluation also, he has to reappear for the same in the next subsequent semester, as and when it is scheduled.

A student shall be given only one time chance to re-register for a maximum of two subjects in a semester:

- If the internal marks secured by a student in the Continuous Internal Evaluation marks for 40 (Sum of average of two mid-term examinations consisting of Objective & descriptive parts, Average of two Assignments & Subject Viva-voce/PPT/ Poster presentation/ Case Study on a topic in the concerned subject) are less than 35% and failed in those subjects.

A student must re-register for the failed subject(s) for 40 marks within four weeks of commencement of the class work in next academic year.

In the event of the student taking this chance, his Continuous Internal Evaluation marks for 40 and Semester End Examination marks for 60 obtained in the previous attempt stand cancelled.

Grading Procedure

Grades will be awarded to indicate the performance of students in each Theory Subject, Laboratory/Practicals/ Industry-Oriented Mini Project/Internship/SDC and Project Stage. Based on the percentage of marks obtained (Continuous Internal Evaluation plus Semester End Examination, both taken together) as specified in item 8 above, a corresponding letter grade shall be given.

As a measure of the performance of a student, a 10-point absolute grading system using the following letter grades (as per UGC/AICTE guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured in a Subject/Course (Class Intervals)	Letter Grade (UGC Guidelines)	Grade Points
Greater than or equal to 90%	O (Outstanding)	10
80 and less than 90%	A ⁺ (Excellent)	9
70 and less than 80%	A (Very Good)	8
60 and less than 70%	B ⁺ (Good)	7
50 and less than 60%	B (Average)	6
40 and less than 50%	C (Pass)	5
Below 40%	F (FAIL)	0

Absent	Ab	0
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A student who has obtained an „F’ grade in any subject shall be deemed to have „**failed**’ and is required to reappear as a „supplementary student” in the semester end examination, as and when offered. In such cases, internal marks in those subjects will remain the same as those obtained earlier.

To a student who has not appeared for an examination in any subject, „Ab’ grade will be allocated in that subject, and he is deemed to have „**Failed**’. A student will be required to reappear as a „supplementary student” in the semester end examination, as and when offered next. In this case also, the internal marks in those subjects will remain the same as those obtained earlier.

A letter grade does not indicate any specific percentage of marks secured by the student, but it indicates only the range of percentage of marks.

A student earns Grade Point (GP) in each subject/ course, on the basis of the letter grade secured in that subject/ course. The corresponding „Credit Points” (CP) are computed by multiplying the grade point with credits for that particular subject/ course.

Credit Points (CP) = Grade Point (GP) x Credits For a course

A student passes the subject/ course only when **GP ≥ 5** (‘C’ grade or above)

The Semester Grade Point Average (SGPA) is calculated by dividing the sum of credit points (ΣCP) secured from all subjects/ courses registered in a semester, by the total number of credits registered during that semester. SGPA is rounded off to **two** decimal places. SGPA is thus computed as

$$\text{SGPA} = \{ \sum_{i=1}^N C_i G_i \} / \{ \sum_{i=1}^N C_i \} \dots \text{For each semester,}$$

where „i” is the subject indicator index (considering all subjects in a semester), „N” is the no. of subjects „**registered**’ for the semester (as specifically required and listed under the course structure of the parent department), C_i is the no. of credits allotted to the i^{th} subject, and G_i represents the grade points (GP) corresponding to the letter grade awarded for that i^{th} subject.

The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student in all semesters considered for registration. The CGPA is the ratio of the total credit points secured by a student in **all** registered courses (of 160) in **all** semesters, and the total number of credits registered in **all** the semesters. CGPA is rounded off to **two** decimal places. CGPA is thus computed from the I year II semester onwards at the end of each semester as per the formula

$$\text{CGPA} = \{ \sum_{j=1}^M C_j G_j \} / \{ \sum_{j=1}^M C_j \} \dots \text{for all S semesters registered}$$

$$j=1$$

$$j=1$$

(i.e., up to and inclusive of S semesters, $S \geq 2$),

where „M’ is the **total** no. of subjects (as specifically required and listed under the course structure of the parent department) the student has „**registered**’ i.e., from the 1st semester onwards up to and inclusive of the 8th semester, „j’’ is the subject indicator index (takes into account all subjects from 1 to 8 semesters), C_j is the no. of credits allotted to the jth subject, and G_j represents the grade points (GP) corresponding to the letter grade awarded for that jth subject. After registration and completion of I year I semester, the SGPA of that semester itself may be taken as the CGPA, as there are no cumulative effects.

Illustration of calculation of SGPA:

Course/ Subject	Credits	Letter Grade	Grade Points	Credit Points
Course 1	4	A	8	$4 \times 8 = 32$
Course 2	4	O	10	$4 \times 10 = 40$
Course 3	4	C	5	$4 \times 5 = 20$
Course 4	3	B	6	$3 \times 6 = 18$
Course 5	3	A+	9	$3 \times 9 = 27$
Course 6	3	C	5	$3 \times 5 = 15$
	21			152

$$SGPA = 152/21 = 7.24$$

Illustration of Calculation of CGPA up to 3rd Semester:

Semester	Course / Subject Title	Credits Allotted	Letter Grade Secured	Corresponding Grade Point (GP)	Credit Points (CP)
I	Course 1	3	A	8	24
I	Course 2	3	O	10	30
I	Course 3	3	B	6	18
I	Course 4	4	A	8	32
I	Course 5	3	A+	9	27
I	Course 6	4	C	5	20
II	Course 7	4	B	6	24
II	Course 8	4	A	8	32
II	Course 9	3	C	5	15
II	Course 10	3	O	10	30
II	Course 11	3	B+	7	21
II	Course 12	4	B	6	24
II	Course 13	4	A	8	32
II	Course 14	3	O	10	30
III	Course 15	2	A	8	16

III	Course 16	1	C	5	5
III	Course 17	4	O	10	40
III	Course 18	3	B+	7	21
III	Course 19	4	B	6	24
III	Course 20	4	A	8	32
III	Course 21	3	B+	7	21
	Total Credits	69		Total Credit Points	518

$$\text{CGPA} = 518/69 = 7.51$$

The calculation process of CGPA illustrated above will be followed for each subsequent semester until 8th semester. The CGPA obtained at the end of 8th semester will become the final CGPA secured for entire B.Tech. Programme.

For merit ranking or comparison purposes or any other listing, **only** the „rounded off” values of the CGPAs will be used.

SGPA and CGPA of a semester will be mentioned in the semester Memorandum of Grades if all subjects of that semester are passed in first attempt. Otherwise the SGPA and CGPA shall be mentioned only on the Memorandum of Grades in which sitting he passed his last exam in that semester. However, mandatory courses will not be taken into consideration.

Passing Standards

A student shall be declared successful or „passed” in a semester, if he secures a GP ≥ 5 (‘C’ grade or above) in every subject/course in that semester (i.e. when the student gets an SGPA ≥ 5.0 at the end of that particular semester); and he shall be declared successful or

„passed” in the entire undergraduate programme, only when gets a CGPA

≥ 5.00 (‘C’ grade or above) for the award of the degree as required.

After the completion of each semester, a grade card or grade sheet shall be issued to all the registered students of that semester, indicating the letter grades and credits earned. It will show the details of the courses registered (course code, title, no. of credits, grade earned, etc.) and credits earned. **There is NO exemption of credits in any case.**

Declaration of results

Computation of SGPA and CGPA are done using the procedure listed in 9.6 to 9.9.

For final percentage of marks equivalent to the computed final CGPA, the following formula may be used.

$$\% \text{ of Marks} = (\text{final CGPA} - 0.5) \times 10$$

Award of Degree

A student who registers for all the specified subjects/ courses as listed in the course structure and secures the required number of 160 credits (with CGPA ≥ 5.0), within 8 academic years from the date of commencement of the first academic year, shall be declared to have „**qualified**’ for the award of B.Tech. degree in the branch of Engineering selected at the time of admission.

A student who qualifies for the award of the degree as listed in item 12.1 shall be placed in the following classes.

A student with final CGPA (at the end of the undergraduate programme) > 8.00 , and fulfilling the following conditions - shall be placed in „**First Class with Distinction**’.

However, he

- (i) Should have passed all the subjects/courses in „**First Appearance**’ within the first 4 academic years (or 8 sequential semesters) from the date of

commencement of first year first semester.

- (ii) Should not have been detained or prevented from writing the semester end examinations in any semester due to shortage of attendance or any other reason.

A student not fulfilling any of the above conditions with final CGPA > 8 shall be placed in '**First Class**'.

Students with final CGPA (at the end of the undergraduate programme) ≥ 7.0 but < 8.00 shall be placed in '**First Class**'.

Students with final CGPA (at the end of the undergraduate programme) ≥ 6.00 but < 7.00 , shall be placed in „**Second Class**'.

All other students who qualify for the award of the degree (as per item 12.1), with final CGPA (at the end of the undergraduate programme) ≥ 5.00 but < 6 , shall be placed in „**pass class**".

A student with final CGPA (at the end of the undergraduate programme) < 5.00 will not be eligible for the award of the degree.

Students fulfilling the conditions listed under item 12.3 alone will be eligible for award of „**Gold Medal**".

Award of 2-Year B.Tech. Diploma Certificate

1. A student is awarded 2-Year UG Diploma Certificate in the concerned engineering branch on completion of all the academic requirements and earned all the 80 credits (within 4 years from the date of admission) upto B.Tech. II Year II Semester, if the student want to exit the 4-Year B.Tech. Program and *requests for the 2 -Year B. Tech. (UG) Diploma Certificate*.
2. The student **once opted and awarded 2-Year UG Diploma Certificate, the student will be permitted to join** in B. Tech. III Year I Semester and continue for completion of remaining years of study for 4-Year B. Tech. Degree ONLY in the next academic year along with next batch students. *However, if any student wishes to continue the study after opting for exit, he/she should register for the subjects/courses in III Year I Semester before commencement of class work for that semester.*
3. *The students, who exit the 4-Year B. Tech. program after II Year of study and wish to re-join the B.Tech. program, must submit the 2 -Year B. Tech. (UG) Diploma Certificate awarded to him, subject to the eligibility for completion of Course/Degree.*
4. A student may be permitted to take one year break after completion of II Year II Semester or B. Tech. III Year II Semester (with university permission through the principal of the college well in advance) and can re-enter the course in **next Academic Year in the same college** and complete the course on fulfilling all the

academic credentials within a stipulated duration i.e. double the duration of the course (Ex. within 8 Years for 4-Year program).

Withholding of results

If the student has not paid the fees to the University at any stage, or has dues pending due to any reason whatsoever, or if any case of indiscipline is pending, the result of the student may be withheld, and the student will not be allowed to go into the next higher semester. The award or issue of the degree may also be withheld in such cases.

Transitory Regulations

A. For students detained due to shortage of attendance:

1. A Student who has been detained in I year of R20 Regulations due to lack of attendance, shall be permitted to join I year I Semester of R22 Regulations and he is required to complete the study of B.Tech. Programme within the stipulated period of eight academic years from the date of first admission in I Year.
2. A student who has been detained in any semester of II, III and IV years of R20 regulations for want of attendance, shall be permitted to join the corresponding semester of R22 Regulations and is required to complete the study of B.Tech. within the stipulated period of eight academic years from the date of first admission in I Year. The R22 Academic Regulations under which a student has been readmitted shall be applicable to that student from that semester. See rule (C) for further Transitory Regulations.

B. For students detained due to shortage of credits:

3. A student of R20 Regulations, who has been detained due to lack of credits, shall be promoted to the next semester of R22 Regulations only after acquiring the required number of credits as per the corresponding regulations of his/her first admission. The total credits required are 160 including both R20 & R22 regulations. The student is required to complete the study of B.Tech. within the stipulated period of eight academic years from the year of first admission. The R22 Academic Regulations are applicable to a student from the year of readmission. See rule (C) for further Transitory Regulations.

C. For readmitted students in R22 Regulations:

4. A student who has failed in any subject under any regulation has to pass those subjects in the same regulations.
5. The maximum credits that a student acquires for the award of degree, shall be the sum of the total number of credits secured in all the regulations of his/her study including R22 Regulations. **There is NO exemption of credits in any case.**
6. If a student is readmitted to R22 Regulations and has any subject with 80% of syllabus common with his/her previous regulations, that particular subject in R22 Regulations will be substituted by another subject to be suggested by the University.

Note: If a student readmitted to R22 Regulations and has not studied any subjects/topics in his/her earlier regulations of study which is prerequisite for further subjects in R22 Regulations, the College Principals concerned shall conduct remedial classes to cover

those subjects/topics for the benefit of the students.

Student Transfers

There shall be no branch transfers after the completion of admission process.

There shall be no transfers from one college/stream to another within the constituent colleges and units of Jawaharlal Nehru Technological University Hyderabad.

The students seeking transfer to colleges affiliated to JNTUH from various other Universities/institutions have to pass the failed subjects which are equivalent to the subjects of JNTUH, and also pass the subjects of JNTUH which the students have not studied at the earlier institution. Further, though the students have passed some of the subjects at the earlier institutions, if the same subjects are prescribed in different semesters of JNTUH, the students have to study those subjects in JNTUH in spite of the fact that those subjects are repeated.

The transferred students from other Universities/Institutions to JNTUH affiliated colleges who are on rolls are to be provided one chance to write the CBT (for internal marks) in the **equivalent subject(s)** as per the clearance letter issued by the University.

The autonomous affiliated colleges have to provide one chance to write the internal examinations in the **equivalent subject(s)** to the students transferred from other universities/institutions to JNTUH autonomous affiliated colleges who are on rolls, as per the clearance (equivalence) letter issued by the University.

Scope

The academic regulations should be read as a whole, for the purpose of any interpretation.

In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.

The University may change or amend the academic regulations, course structure or syllabi at any time, and the changes or amendments made shall be applicable to all students with effect from the dates notified by the University authorities.

Where the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

**ACADEMIC REGULATIONS FOR B.TECH (LATERAL ENTRY SCHEME) FROM
THE AY 2023-24**

1. Eligibility for the award of B.Tech Degree (LES)

The LES students after securing admission shall pursue a course of study for not less than three academic years and not more than six academic years.

2. The student shall register for 120 credits and secure 120 credits with CGPA ≥ 5 from II year to IV-year B.Tech. Programme (LES) for the award of B.Tech. Degree.
3. The students, who fail to fulfil the requirement for the award of the degree in six academic years from the year of admission, shall forfeit their seat in B.Tech.
4. The attendance requirements of B. Tech. (Regular) shall be applicable to B.Tech. (LES).

5. Promotion rule

S. No	Promotion	Conditions to be fulfilled
1	Second year first semester to second year second semester	Regular course of study of second year first semester.
2	Second year second semester to third year first semester	(i) Regular course of study of second year second semester. (ii) Must have secured at least 24 credits out of 40 credits i.e., 60% credits up to second year second semester from all the relevant regular and supplementary examinations, whether the student takes those examinations or not.
3	Third year first semester to third year second semester	Regular course of study of third year first semester.
4	Third year second semester to fourth year first semester	(i) Regular course of study of third year second semester. (ii) Must have secured at least 48 credits out of 80 credits i.e., 60% credits up to third year second semester from all the relevant regular and supplementary examinations, whether the student takes those examinations or not.
5	Fourth year first semester to fourth year second semester	Regular course of study of fourth year first semester.

6. All the other regulations as applicable to B. Tech. 4-year degree course (Regular) will hold good for B. Tech. (Lateral Entry Scheme).
7. LES students are not eligible for 2-Year B. Tech. Diploma Certificate.

Malpractices Rules

Disciplinary Action For / Improper Conduct in Examinations

	Nature of Malpractices/Improper conduct	Punishment
	If the student:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which student is appearing but has not made use of (material shall include any marks on the body of the student which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other student orally or by any other body language methods or communicates through cell phones with any student or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the students involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the student is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The hall ticket of the student is to be cancelled and sent to the University.
3.	Impersonates any other student in connection with the examination.	The student who has impersonated shall be expelled from examination hall. The student is also debarred and forfeits the seat. The performance of the original student who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for

		examinations of the remaining subjects of that semester/year. The student is also debarred for two consecutive
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		semesters from class work and all University examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the chief superintendent/assistant – superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the student(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The students also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.

	part of the college campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	
7.	Leaves the exam hall taking away answer script or intentionally tears off the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the student is subject to the academic regulations in connection with forfeiture of seat.
8.	Possesses any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred and forfeits the seat.
9.	If student of the college, who is not a student for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The student is also debarred and forfeits the seat. Person(s) who do not belong to the college will be handed over to the police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the student has already appeared for including practical examinations and project work and shall not be permitted for

		the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the student has appeared for including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award a suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the students as per the above guidelines.
2. Punishment for Institutions: (if the squad reports that the college is also involved in encouraging malpractices)
 - a. A show-cause notice shall be issued to the college.
 - b. Impose a suitable fine on the college.
 - c. Shifting the examination center from one college to another college for a specific period of not less than one year.

ACADEMIC CALENDER (2024-25)

II & III B.Tech. I – SEMISTER				
S. No.	EVENT	DATE		DURATION
		FROM	TO	
		29.07.2024		---
1	Commencement of Class Work			
2	First Spell of Instructions	29.07.2024	21.09.2024	8 weeks
3	First Mid Term Examinations (Theory & Practical)	23.09.2024	28.09.2024	1 Week
4	Second Spell of Instructions (Including Dussehra Vacation)*	30.09.2024	30.11.2024	9 weeks
5	Submission of First Mid Term Marks to Exam Branch	05.10.2024		---
6	Parents Teacher's Meeting	14.10.2024		---
7	Second Mid Term Examinations (Theory & Practical)	02.12.2024	07.12.2024	1 Week
8	Submission of Second Mid Term Marks to Exam Branch	14.12.2024		---
9	Preparation Holidays and Practical Examinations	09.12.2024	14.12.2024	1 week
10	End Semester & Supplementary Examinations	16.12.2024	28.12.2024	2 Weeks
II & III B.Tech. II – Semester				
S. No.	EVENT	DATE		DURATION
		FROM	TO	
		30.12.2024		---
1	Commencement of II-SEM Class work			
2	First Spell of Instructions	30.12.2024	22.02.2025	8 weeks
3	First Mid Term Examinations	24.02.2025	01.03.2025	1 week
4	Second Spell of Instructions	03.03.2025	26.04.2025	8 weeks
5	Submission of First Mid Term Marks to Exam Branch	08.03.2025		---
6	Parents Teacher's Meeting	15.03.2025		---
7	Second Mid Term Examinations	28.04.2025	03.05.2025	1 week
8	Summer Vacation	05.05.2025	31.05.2025	4 weeks
9	Submission of Second Mid Term Marks to Exam Branch	14.06.2025		---
10	Preparation and Practical Examinations	02.06.2025	07.06.2025	1 week
11	End Semester & Supplementary Examinations	09.06.2025	21.06.2025	2 weeks
12	Commencement of Class Work for the next A.Y-2025-2026	30.06.2025		

S.NO	DATE	NAME OF THE EVENT
1	29/07/2024	Commencement of Class Work
2	29/07/2024-21/09/2024	I Spell of instructions
3	02/08/2024-03/08/2024	IV B.Tech Mini Project Work Review I
4	07/08/2024	Student Workshop-I for IV Year
5	06/09/2024	Student Workshop-I for III Year
6	07/08/2024	Industrial visit
6	07/09/2024 - 08/09/2024	IV B.Tech Mini Project Work Review II
7	09/09/2024 - 12/09/2024	I MID Exams for IV Year
8	30/09/2024-03/10/2024	I MID Lab Internal Exam for IV Years
9	13/09/2024 - 14/09/2024	IV B.Tech Major Project Work Review I
10	14/09/2024	Guest lecture for III year
11	27/09/2024 - 28/09/2024	IV B.Tech Mini Project Work Review II
12	30/09/2024-05/10/2024	I MID Exams for II & III Years
13	30/09/2024-03/10/2024	I MID Lab Internal Exam for II, & III Years
14	05/10/2024	Submission of I mid marks to University
15	16/09/2024	Professional Body Activities
16	07/10/2024-12/10/2024	Dussehra Recess
17	30/09/2024-30/11/2024	II Spell of instructions (Including I mid examinations)
18	30/09/2024-05/10/2024	I MID Exams for II, III & IV Years
19	30/09/2024-03/10/2024	I MID Lab Internal Exam for II, & III Years
20	05/10/2024	Submission of I mid marks to University
21	21/10/2024 - 22/10/2024	IV B.Tech Mini Project Work Review III
22	11/11/2024 - 16/11/2024	II MID Exams for IV Years
23	12/11/2024	Workshop for II year
24	15/11/2024 - 16/11/2024	IV B.Tech Major Project Work Review II
25	28/11/2024 - 30/11/2024	II MID Lab Internal Exam for II, & III Years
26	02/12/2024 - 07/12/2024	II MID Exams for II&III Years
27	09/12/2024 - 11/12/2024	Lab External Exam for IV Year
28	09/12/2024 - 11/12/2024	Lab External Exam for II, & III Years
29	09/12/2024 - 14/12/2024	Preparation Holidays and Practical Examinations
30	14/12/2024	Submission of II mid marks to University
31	16/12/2024 -28/12/2024	End Semester Exams

Department Event Planner A.Y 2024-2025

LIST OF SUBJECTS:

1	Antenna and wave processing
2	Digital Signal Processing
3	VLSI Design

4	Professional Elective-II
5	Open Elective-I
6	Digital Signal Processing Lab
7	Internet of Things Lab
8	Industry Oriented Mini Project/Internship
9	Intellectual Property rights

Subject: Antenna and wave propagation

Subject: ANTENNAS AND WAVE PROPOGATION

Year: III– B.Tech, II SEM

Branch: ECE

A.Y:2024-25

ACADEMIC PLANNER

Subject:

<u>S.NO</u>	<u>CONTENT</u>
(1) -	Preamble/Introduction
(2) -	Prerequisites
(3) -	Objectives and Outcomes
(4) -	Syllabus 1.R22-CMREC 2.GATE 3.IES
(5) -	List of Expert Details (Local/National/International with Contact details/Profile link/Blogs/their research Contribution towards the subject)
(6) -	Journals with min 5 ref paper for literature study
(7) -	Subject -Lesson plan
(8) -	Suggested Books (prescribed and References)
(9) -	Websites for self learning Resources like <i>www.geeksforgeeks.org, www.schools.com, Coursera ,edX, Udemy, Khan Academy, NPTEL etc along Registration procedures)</i>
(10) -	Question Banks 1.JNTUH/Model papers 2.GATE
(11) -	Two case study presentations with Project / Product/ Model /prototypes/ Industrial applications.
(12) -	Assignment Question/Innovative Assignments sets.
(13) -	List of topics for students Seminars with Guidelines
(14) -	STEP/Course material in softcopy
(15) -	Expert Lectures with topics & Schedules(if any)

1.Introduction:

An antenna is a metallic structure that captures and/or transmits radio electromagnetic waves from/ or into the free space. Here different types of antennas like Dipole, Loop, Helical, Horn, Yagi-Uda, Micro strip patch, Reflector, Array Antennas are discussed. Also discussed about different types of wave propagation.

2. Prerequisites

- ✓ Knowledge of basics of electromagnetic wave theory
- ✓ Acceleration and deceleration of charges and radiation
- ✓ Circuit behavior of transmission line and its primary and secondary parameters and their changes along the length of the line .

3.Objectives:

1. To understand the concept of radiation, antenna definitions and significance of antenna parameters, to derive and analyze the radiation characteristics of thin wire dipole antennas and solve numerical problems.
2. To analyze the characteristics and design relations of UHF, VHF and Microwave Antennas.
3. To identify the antenna array requirements, to determine the characteristics of ULAs and estimate the patterns of BSA, EFA, and Binomial Arrays.
4. To understand the concepts and set-up requirements for microwave measurements, and familiarize with the procedure to enable antenna measurements.
5. To define and distinguish between different phenomenon of wave propagation (ground wave, space wave and sky wave), their frequency dependence, and estimate their characteristics, identifying their profiles and parameters involved.

SCOPE

- Knowledge applied in Telecommunication, TV broadcasting, DTH, Satellite communication, Wireless communication

4. SYLLABUS:(R22)

UNIT:1

Antenna basics: introduction, basic antenna parameters-patterns, beam area, radiation intensity, beam efficiency, directivity/gain resolution, antenna aperture, effective height, illustrative problems. Fields from oscillating dipole, field zones, shape: impedance considerations, antenna temperature, front to back ratio, antenna theorems, radiation: basic max well equations retarded potentials: Helmholtz theorem.

Thin linear wire antennas- radiation from small electric dipole, quarter wave monopole and half wave dipole-current distributions, field comparisons, radiated power, radiation resistance, beam width, directivity, effective area and effective height, natural current distributions, far fields and patterns of thin linear centre fed antennas of different lengths, illustrative problems. Loop antennas-introduction, small loop, comparison of far fields of small loop and short dipole, radiation resistance and directivities of small and large loops(qualitative treatment)

UNIT:II

Antenna arrays: Point Sources- Definition, Patterns, arrays of 2 Isotropic Sources Different Cases, Principle of patterns Multiplication, uniform Linear Arrays – Broadside Arrays, End fire Arrays, EFA with Increased Directivity, Derivation of their Characteristics and Comparison, BSAs with Non-uniform Amplitude Distributions-General Considerations and Binomial Arrays, Illustrative problems. Antenna Measurements: Introduction, Concepts - Reciprocity, Near and Far Fields, Coordinate System, Sources of Errors. Patterns to be Measured, Directivity Measurement, Gain Measurements (by Comparison, Absolute and 3-Antenna Methods)

UNIT:III- VHF, UHF, MICROWAVE ANTENNAS:I

Arrays with parasitic elements, yagi-uda array, folded dipoles and their characteristics, helical antennas-helical geometry, helix modes, practical design considerations for monofilar helical antenna in axial and normal modes. Horn antennas-types, Fermat's principle, optimum horns, design considerations of pyramidal horns, illustrative problems.

UNIT: IV- VHF, UHF, MICROWAVE ANTENNAS-II

Micro strip antennas-introduction, features, adv and limitations, rectangular patch antennas-geometry and parameters, characteristics of micro strip antennas. Impact of different parameters on characteristics, reflector antenna-introduction, flat sheet and corner reflectors, parabolic reflector-geometry ,pattern characteristics, feed methods, reflector types-related features, illustrative problems.

UNIT:V

Wave propagation1: Introduction, definitions, categorization and general classifications, different modes of wave propagation, ray/mode concepts,

Ground wave propagation- introduction, plane earth reflections, space and surface waves, wave tilt, curved earth reflections .

Space wave propagation- introduction, field strength variation with distance and height, effect of earth's curvature, absorption. Super refraction, m-curves and duct propagation, scattering phenomena, troposphere propagation, fading and path loss calculations.

Sky wave propagation-introduction, structure of ionosphere, refraction and reflection of sky wave by ionosphere, ray path, critical frequency, MUF,LUF,OF,Virtual height and skip distance, relation between MUF,and skip distance, multichop propagation.

2. GATE :SYLLABUS

Dipole and monopole antennas, linear antenna arrays.

3. SYLLABUS – IES

Antennas-radiation pattern, monopoles/dipoles, gain, arrays-active/passive, theory, uses.

Suggested Books

TEXT BOOKS

T1. Antennas and wave propagation-J.D.kraus, R.J.Marhefka and Ahmad S.khan, TMH, New Delhi, 4th edition,(special indian edition) 2010.

T2.Electromagnetic wave and radiating systems-E.C.Jordan and k.g.balmain,phi,2nd ,edition 2000.

REFERENCE BOOKS

- R1. Antenna Theory-C.A.Balanis, Johnwiley And Sons, 3rd , Edition,2005.
- R2.Antenna And Wave Propagation-K.D.Prasad,SatyaPrakashan Tech India Publications, New Delhi ,2001.
- R3. Radio Engineering Handbook- Keith henney, 3rd edition TMH.
- R4. Antenna Engineering Handbook –John Leonidas Volakis, 3rd edition, 2007

Websites

- <https://www.youtube.com/watch?v=-5AcIZYxdw8&list=PLgwJf8NK-2e7tzLIDL4aXUbtRFY3ykmkT> - Engineering Funda (Antenna Parameters)
- https://www.youtube.com/results?search_query=halfwave+dipole (Halfwave dipole)
- <https://www.youtube.com/playlist?list=PL3UZlxOnyu9CRoBFsG5x-VqYeC69FmMZT> -NPTEL Videos
- <https://www.youtube.com/watch?v=HH58VmUbOKM> – Khan Academy (polarization)
-
- www.ieee.org
- <http://nptel.ac.in>
- www.educyclopedia.be/electronic/digital.com
- www.iitb.ac.in
- www.iitm.ac.in
- www.iitr.ac.in
- www.iitg.ernet.in
- www.bits-pilani.ac.in
- www.iisc.ernet.in
- www.samsung.com
- www.vedaiit.com

5. Expert Details

International

- Dr.A Alphones, Associate Professor, Nanyang Technological University,Singapore.
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- Dr.B. Manimegalai , Professor in ECE, Thiagarajar College of Engineering.
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- Dr. Sukomal Dey, Assistant Professor , IIT Palakkad

Regional:

- Dr. N.S.Murthy, Professor and Head Dept. of ECE, NIT, Warangal - 506004 (India) email: nsm@recw.ernet.in

6. JOURNALS

- 1.International Journal of Antennas and wave propagation
2. International Journal of Electromagnitics
- 3 .IEEE magazine
- 4.Educational journal of IETE

Samples:

- Analysis of impedance matching stair-shaped slot antenna for 60 GHz femtocell applications
- Analysis of impedance matching stair-shaped slot antenna for 60 GHz femtocell applications

7. Teaching Schedule/Lesson plan

S.NO	TOPIC TO BE COVERED	Suggested Books (Eg. T1, T2,R5)	NO. OF LECTURES REQUIRED
	UNIT - I		
1.	Antenna basics: introduction, basic antenna parameters-patterns, beam area,	T1,T2,R1,R2	L1
2.	Radiation Intensity, Beam Efficiency, Directivity/Gain Resolution,	T1,T2,R1,R2	L2,L3
3.	Antenna aperture, effective height,. Fields from oscillating dipole, field zones, Front to back ratio	T1,T2,R1,R2	L4
4	Antenna Theroms,Radiation:Basic Max WellEquations retarded potentials:helmholtz theorem.	T1,T2,R1,R2	L5,L6
5	Illustrative Problems	T1,T2,R1,R2	L7
6	Thin linear wire antennas-radiation from small electric dipole	T1,T2,R1,R2	L8

7	Quarter wave monopole	T1,T2,R1,R2	L9
8	half wave dipole-current distributions	T1,T2,R1,R2	L10
9	Field comparisons, Radiated power, radiation resistance	T1,T2,R1,R2	L11
10	Beam width, directivity, effective area	T1,T2,R1,R2	L12
11	effective height, natural current distributions	T1,T2,R1,R2	L13
12	Far fields and patterns of thin linear centre fed antennas of different lengths	T1,T2,R1,R2	L14
13	Loop antennas-introduction, Small loop	T1,T2,R1,R2	L15
14	Comparison of far fields of small loop and short dipole	T1,T2,R1,R2	L16
15	Radiation resistance and directives of small and large loops(qualitative treatment	T1,T2,R1,R2	L17
16	Illustrative problems	T1,T2,R1,R2T1	L18
	UNIT-II		
17	Antenna arrays: Point Sources-Definition, Patterns	T1,T2,R1,R2	L19
18	Arrays of 2 Isotropic Sources Different Cases	T1,T2,R1,R2	L20
19	Principle of patterns Multiplication,	T1,T2,R1,R2	L21
20	uniform Liners Arrays – Broadside Arrays	T1,T2,R1,R2	L22
21	End fire Arrays	T1,T2,R1,R2	L23
22	EFA with Increased Directivity	T1,T2,R1,R2	L24
23	Derivation of their Characteristics and Comparison	T1,T2,R1,R2	L25
24	BSAs with Non-uniform Amplitude	T1,T2,R1,R2	L26
25	Distributions-General Considerations and Binomials Arrays.	T1,T2,R1,R2	L27
26	illustrative problems	T1,T2,R1,R2	L28
	Antenna measurements: introduction, concepts-reciprocity,near and far fields	T1,T2,R1,R2	L29
	Coordinate system, source of errors	T1,T2,R1,R2	L30
	Patterns to be measured, pattern measurement arrangement	T1,T2,R1,R2	L31

	Directivity measurement	T1,T2,R1,R2	L32
	Gain measurement(by comparison, absolute and 3-antenna methods.) Illustrative Problems	T1,T2,R1,R2	L33
	UNIT-III		
27	VHF,UHF,MICROWAVE ANTENNAS:1- arrays with parasitic elements	T1,T2,R1,R2	L34
28	Yagi-udaarray,folded dipoles and their characteristics	T1,T2,R1,R2	L35,L36
29	helical antennas-helical geometry,Helix modes	T1,T2,R1,R2	L37,L38
30	Practical design considerations for monofilar helical antenna in axial and normal modes.	T1,T2,R1,R2	L39
31	Hornantennas-types,fermat's principal,	T1,T2,R1,R2	L40
32	Optimum horns, design considerations of pyramidal horns,	T1,T2,R1,R2	L41
	UNIT-IV		
34	VHF,UHF,MICROWAVE ANTENNA-ii- micro strip antennas-introduction	T1,T2,R1,R2	L41
35	Features, adv and limitations, rectangular patch	T1,T2,R1,R2	L42
36	Antennas-geometry and parameters, characteristics of micro strip antennas	T1,T2,R1,R2	L43
37	impact of different parameters on characteristics,	T1,T2,R1,R2	L44
38	Reflector antenna-introduction,flat sheet and corner reflectors	T1,T2,R1,R2	L45
39	parabolicreflector-geometry,pattern characteristics	T1,T2,R1,R2	L46
40	Feed methods, reflector types-related features	T1,T2,R1,R2	L47
41	Illustrative problems	T1,T2,R1,R2	L48
	UNIT-V		
49	Introduction, definitions, categorization and general classifications	T1,R2	L49
50	Different modes of wave propagation , Ray/mode concepts	T1,R2	L50
51	Ground wave propagation introduction, plane earth reflections,	T1,R2	L51
52	Space and surface waves, wave tilt,	T1,R2	L52

	curved earth reflections		
53	space wave propagation -introduction, field strength variation with distance and height	T1,R2	L53
54	Effect of earth's curvature, absorption. Super refraction, m-curves and duct propagation	T1,R2	L54
55	scattering phenomena, troposphere propagation, fading and path loss calculations	T1, R2,R4	L55
56	Sky wave propagation -introduction, Structure of ionosphere	T1, R2	L56
57	Refraction and reflection of sky wave by ionosphere	T1, R2	L57
58	Ray path, critical frequency, MUF, LUF, OF, frequency ranges.	T1, R2	L58,L59
59	height and skip distance, Relation between MUF,and skip distance	T1, R2	L60
60	Multihop propagation	T1, R2	L61

COURSE OUTCOMES:

Antenna and wave propagation Course Outcomes
<ul style="list-style-type: none"> • CO1: Explain the basic principles of radiation and the fundamentals of antenna parameters such as gain, directivity, and radiation pattern. • CO2: Analyze the performance of various antenna types such as dipole, loop, and aperture antennas for specific applications. • CO3: Explain the setup and instrumentation required for measuring key antenna parameters and Calculate the antenna parameters • CO4: Design the antennas to meet specific requirements in terms of frequency, bandwidth, and radiation characteristics. • CO5: Understand the basic concepts of wave propagation & Evaluate the propagation characteristics of electromagnetic waves in different media.

Question Bank

PREVIOUS QUESTION PAPERS

UNIT:1

1. Derive the relationship between directivity and effective area, directivity and effective length.
2. Define
 - 1) Radiation Intensity, ii) Beam Area, iii) Effective Height and iv) Resolution
3. Define and explain Directivity and Power Gain of an Antenna. Prove that the directivity of a half wave dipole is 2.15dB.
4. What are principle planes? How the Antenna Beam Width is defined in such planes
5. Define and explain the following terms.
 - i). Gain ii).Directivity iii). Radiation Resistance iv). Bandwidth
- 6 Define the following terms:
 - i) Gain. ii) Directivity iii) Radiation resistance iv)Effectivearea.
7. Derive the relationship between Directive Gain, Radiation Resistance and Effective Length.
8. Define the terms electrostatic field, induction field, and radiation field of an antenna and bring out their significance
9. Mention the frequency ranges of operation and applications of
 - i) Loop antenna
 - ii) Helical antenna
 - iii) Lens antenna.
10. Derive the EMF equation for a small loop antenna.
11. Explain radiation from a quarter wave monopole with sketches.
12. Explain radiation from a quarter wave monopole with sketches.
13. Prove that for a Hertzian dipole, the aperture area is 0.12λ and for a half wave dipole, it is 0.13λ and for an isotropic radiator, it is 0.08λ . Explain relations used.
14. Explain radiation from a quarter wave monopole with sketches.
15. Draw the radiation pattern of an dipole Antenna and explain all its characteristics?
16. Find the radiation resistance and directivity of a circular loop antenna of 20 cm. diameter at a frequency of 100 MHz what happens
 - i) if the loop is changed in to a square loop of same area.
 - ii) If the no. of turns of the circular loop is doubled.
9. What is an elementary doublet? How does it differ from the infinitesimal dipole?
17. 10m high monopole is to be used as a portable transmitting antenna at 1.5MHz. Its measured base reactance is $j350$ ohms with $Q=100$ and ohmic losses in the ground system and turning cost are equal. Find antenna e_{eff} -

ciency, gain of the antenna and its aperture.?

18. Discuss the conditions under which parasitic dipole placed near and parallel to a driven dipole can act as rector?
19. A Hertzian dipole of length $dl=0.5\text{m}$ is radiating into free space. If the dipole current is 4A and the frequency is 10MHz , calculate the highest power density at a distance of 2km from the antenna.
20. Find the field pattern of loop antenna using principle of arrays.
22. Establish the field expressions for a small loop antenna, listing out the assumptions involved, and sketch its pattern?
23. Determine magnitude of E and H of a half wave dipole operated at a frequency of 300 MHz at a distance of 100m in the broad side plane for maximum radiation. Input current to antenna is 100mA . How much average power is radiated by this antenna.

UNIT:2

1. Explain the characteristics and properties of a Broad side array.
 2. An array consists of four identical isotropic sources located at corners of a square having diagonal length $3\sqrt{2}$ and excited with equal current in same phase. Determine the polar diagram of the array in the plane containing the sources.
 3. Why practically Isotropic radiator can not exist?
 4. What are the advantages and disadvantages of binomial array
 5. list out the design relations associated with a rhombic antenna. What are its applications?
 6. what is a uniform linear array and what are its applications
 7. Derive the conditions for the linear array of 'N' isotropic elements to radiate in end-fire and broadside mode and find the first two side lobe levels
 8. What are the various differences between end-fire and broadside arrays
 9. Explain the principle of multiplication of patterns?
 10. Find the radiation pattern for four isotropic elements fed in face, spaced $\lambda/2$ apart by using pattern Multiplication
- LOOP antennas

1. Which primary feed used for the lens antenna? Why?
- 2.a) Mention the frequency ranges of operation and applications of
 - i) Loop antenna
 - ii) Helical antenna
 - iii) Lens antenna
3. With neat sketch explain basic set up and requirements, for antenna pattern measurement
4. how is the field pattern of the "Receiving Antenna" experimentally determined? Explain it with a neat block diagram
5. What are the precautions to be taken while conducting antenna pattern measurements
6. Explain the gain measurement of an antenna by comparison method.
7. Define and explain Directivity and Power Gain of an Antenna. Prove that the directivity of a half wave dipole is 2.15dB.
8. With a neat sketch explain the absolute method of measuring the gain of an antenna
9. Explain the significance, merits and demerits of zoning in lens antennas

UNIT-3

1. How does a parasitic element act when its length is greater than and smaller than λ .
2. Explain the geometry of paraboloidal reflectors?
3. Draw the general structure and radiation pattern of travelling wave antenna and give expression for its electric field strength.
4. Explain how unidirectional pattern is obtained using a properly terminated rhombic antenna?
5. While measuring gain of a horn antenna, the oscillator was set at 9GHz frequency and the attenuation inserted was 9.8dB. Calculate the gain of the horn antenna if the distance between the two horns is 35cm?
6. What is meant by antenna coupling. Derive condition for same.
7. The pyramidal horn is required to have a half power width of 100 in both the vertical and horizontal planes. Determine the dimensions of the horn mouth and the length of the horn in wavelengths, and the directive gain?
8. With neat sketch explain the operation of H-plane horn antenna?
9. Explain travelling wave antenna and draw its radiation pattern.
10. Draw the structure and Explain the principle of working of helical antenna in normal mode.
11. Determine the length L , aperture a and half angles in E and H planes for a pyramidal electromagnetic horn for which the aperture $a = 8\lambda$. The horn is

fed with a rectangular wave guide with TE(10) mode. Take $\delta = 0.1\lambda$ in the E plane and 0.25λ in the H-plane. Calculate the HPBW in both E and H planes, directivity and aperture efficiency?

12. Discuss the characteristics of an optimum horn. Calculate its gain and directivity, when the aperture dimensions are $30\text{cm} \times 41.1\text{cm}$ at 10GHz.
13. what is optimum spacing used in parasitic array? Why
14. Determine the lengths and spacing requirements for a three element YAGI UDA antenna at 500MHz
15. Distinguish between sectorial, pyramidal, and conical horns with sketches. List their applications.
16. Explain in detail the constructional features of helical antenna
17. with a neat diagram describe the principle of working of a three element Yagi-uda antenna.
18. what is the principle of equality of path length? How is it applicable to horn antenna? Obtain an expression for the directivity of pyramidal horn in terms of its aperture dimensions
19. Briefly explain the impedance measurement of a horn antenna by using slotted line method.

UNIT:4

1. Compare the performances of different reflectors?
2. Write the design relations associated with Rhombic antenna. What are its applications?
3. with a neat sketch explain the image formation for the case of 45° corner reflector
4. Write short notes on diffraction effects in plane sheet reflectors
5. Describe the construction and properties of rhombic antenna.
6. What are the advantages of rhombic antenna over single wire antennas
7. Write short notes on Diffraction effects in plane sheet reflectors
8. Evaluate the power gain directing and the required diameter of a paraboloid having a null beam width of 10 degrees at 3 GHz
9. Explain the gain and beam width relations for a parabolic reflector and account for its beam shaping considerations.

UNIT:5

1. Explain the effect of the following on tropospheric wave propagation?
 - (a) radius of curvature of path
 - (b) Earth's radius

(c) Earth's curvature.

2. Explain the effect of atmosphere on space wave propagation?
3. Calculate the maximum wavelength at which propagation is possible by means of a grounded based duct of 100ft high when $\Delta M = 25$.
4. With neat sketch explain basic set up and requirements, for antenna pattern measurement.
5. Discuss the significance and requirement for polarization in surface wave propagation.
6. Discuss about the following
 - a) Duct formation and its significance
 - b) Shadow zone
 - c) Effective earth's radius
 - d) Free space path loss
6. Write a short notes on
 - i). D-layer, ii) Sporadic E-layer, iii) Fading and iv). Atmospheric noise
7. What is LOS propagation? Under what conditions it can exist
8. Explain the formation of inversion layer in the troposphere in the phenomenon of duct propagation
9. Establish the mathematical relations for
 - i). Radio horizon and ii). Radius of curvature of array path for LOS waves
10. Write short note on the following
 - i). M curves and their characteristics
 - ii). Troposcatter propagation of electromagnetic waves
11. Discuss the importance of ground wave propagation for communication
12. What is wave tilt and how does it affect the field strength received at a distance from the transmitter.

Wave propagation-II

1. Describe a method of estimating the height of ionospheric layer?
2. Write short notes on sun spot cycle?
3. Two points on the earth are 1600Km apart and are communicated by means of HF communication. For single hop transmission, the critical frequency at that time is 7.3MHz. Calculate MUF for these two points if the height of the ionospheric layer is 300Km?
4. Write about the following :
 - (a) ionospheric abnormalities.
 - (b) formation of ionospheric layer

5. Explain about following terms
 - i) Maximum of MUF
 - ii) Optimum frequency
6. What is meant by critical frequency? Describe a method to measure it
7. Explain the effects of D-layer in sky wave propagation
8. Distinguish between the terms MUF, LUHF, and Optimum frequency
9. Write a short notes on
 - i). Ionosphere abnormalities
 - ii). Optimum working frequency and LUHF
10. Describe the fading of short wave broadcast signals
11. Describe the salient features of multi hop propagation

11. Case study presentations with Project / Product/ Model /prototypes/ Industrial applications.

- Planning to analyze antenna parameters using HFSS tool

Case Study 1: Design and Optimization of a Yagi-Uda Antenna for TV Broadcasting

Background:

Traditional television broadcast antennas often suffer from signal attenuation and multipath interference. A Yagi-Uda antenna with optimized element spacing can enhance reception and reduce noise.

Methodology:

- A Yagi-Uda antenna with five elements (one reflector, one driven element, and three directors) was designed for UHF band reception (470–700 MHz).
- Theoretical analysis was performed using the NEC (Numerical Electromagnetic Code) software.
- Physical prototypes were tested for signal reception quality in urban and rural environments.

Results:

- The antenna achieved a gain of 10 dBi, significantly improving signal strength.
- Reduced multipath interference due to its directional pattern.
- Effective reception up to 50 km from the broadcast station.

Conclusion:

The study demonstrated that optimizing Yagi-Uda element lengths and spacing significantly improves television signal reception, making it a cost-effective solution for rural areas.

Case Study: Design and Performance Analysis of a Microstrip Patch Antenna for Wireless Communication

Background

Microstrip patch antennas (MPAs) are widely used in wireless communication due to their low profile, lightweight design, and ease of integration with printed circuit boards (PCBs). This case study focuses on designing and analyzing a microstrip patch antenna for 5G applications operating at 28 GHz.

Objectives

- To design a compact and high-gain microstrip patch antenna for 5G mmWave applications.
- To optimize the antenna parameters for improved bandwidth and efficiency.
- To evaluate real-world performance through simulation and fabrication.

Methodology

Design Parameters

- **Operating Frequency:** 28 GHz (5G mmWave band)
- **Substrate Material:** Rogers RT5880 (dielectric constant $\epsilon_r = 2.2$)
- **Patch Shape:** Rectangular with inset feed
- **Substrate Thickness:** 0.8 mm
- **Feeding Technique:** Microstrip line feeding

Simulation and Optimization

- Designed using **HFSS (High-Frequency Structure Simulator)** and **CST Microwave Studio**.
- Optimized the length and width of the patch to match impedance and maximize gain.
- Added a partial ground plane to enhance bandwidth.

12.ASSIGNMENT QUESTIONS

MID-1

Set :1

2. Define all the parameters of antenna
3. Explain the half wave dipole with necessary equations also calculate radiation resistance

4. Explain the n- array source with equal amplitude and phase (BSA case)
5. Explain the Yagi-Uda antenna with neat diagram.
6. A magnetic field strength of $5 \mu \text{ A/m}$ is required at a point $\theta = 90^\circ$, 2 km away from an antenna in free space. Neglecting ohmic loss, how much power must the antenna transmit if it is Hertzian dipole of length $\lambda/25$.

Set :2

1. Explain the Short dipole with necessary equations also calculate radiation resistance
2. Explain the loop antenna with neat diagram
3. Explain the n- array source with equal amplitude and different phase (EFA case)
4. Explain the Folded dipole antenna with neat diagram.
5. Determine the directivity of Short dipole and Half wave dipole antennas.

Set :3

1. Define the parameters of antenna
 (a) Directivity (b) Radiation pattern (c) gain (d) First null beam width
 (e) Effective height
2. Explain the short dipole with necessary equations
3. Calculate radiation resistance of short dipole and half wave dipole antennas
4. Explain the Yagi-Uda antenna with neat diagram.
5. A electric field strength of $10 \mu \text{ v/m}$ is to be measured at an observation point $\theta = 90^\circ$, 500 km away from an half wave dipole antenna oprating at 500 M Hz.
 - a. What is the length of the dipole.
 - b. Calculate the current that must be fed to the antenna.
 - c. Find the total power radiated by the antenna.

MID-II ASSIGNMENT QUESTIONS

Set :1

1. Compare the performances of different reflectors?

1. Mention the frequency ranges of operation and applications of
 - i) Loop antenna ii) Helical antenna iii) Lens antenna

3. Explain the effect of the following on troposphere wave propagation?

(a) radius of curvature of path (b) Earth's radius (c) Earth's curvature

4. Explain about following terms

i) Maximum of MUF ii) Optimum frequency

6. with a neat sketch explain the image formation for the case of 45° corner reflector

Set :2

1. Compare the performances of different reflectors?

2. With neat sketch explain basic set up and requirements, for antenna pattern measurement

3. Explain the effect of atmosphere on space wave propagation?

4. Write a short notes on

i). D-layer, ii) Sporadic E-layer, iii) Fading and iv). Atmospheric noise

5. What is meant by critical frequency? Describe a method to measure it

Set :3

1. With a neat sketch explain the image formation for the case of 45° corner reflector

1. Explain the significance, merits and demerits of zoning in lens antennas

2. Write short note on the following

i). M curves and their characteristics

ii). Troposcatter propagation of electromagnetic waves

3. Distinguish between the terms MUF, LUHF, and Optimum frequency

4. Describe the salient features of multi hop propagation

Set :4

10. Compare the performances of different reflectors?

11. with a neat sketch explain the absolute method of measuring the gain of an antenna

12. Explain the effect of atmosphere on space wave propagation?
13. Describe the fading of short wave broadcast signals
14. Explain the effects of D-layer in sky wave propagation

STUDENT SEMINAR Topics

- Comparative Study of Antenna Designs for RF Energy Harvesting
- Microstrip Antennas: Future Trends and New Applications
- Reconfigured and Notched Tapered Slot UWB Antenna for Cognitive Radio Applications
- An Efficient Analysis Method for Cylindrical Conformal Microstrip Antenna Fed by Microstripline
- Adaptive Forming of the Beam Pattern of Microstrip Antenna with the Use of an Artificial Neural Network
- Rapid Beam Forming in Smart Antennas Using Smart-Fractal Concepts Employing Combinational Approach Algorithms
- Design of RFID Reader Antenna for Exclusively Reading Single One in Tag Assembling Production
- Compact MIMO Microstrip Antennas for USB Dongle Operating in 2.5–2.7 GHz Frequency Band
- Harmonic Suppressed Slot Antennas Using Rectangular/Circular Defected Ground Structure
- Hybrid Dielectric Resonator Antenna Composed of High-Permittivity Dielectric Resonator for Wireless Communications in WLAN and WiMAX,
- Design and Analysis of a Novel Compact Wideband Antenna with Two Excited Modes
- A Novel Low RCS Design Method for X-Band Vivaldi Antenna
- Novel Compact CPW-Fed Antennas with Harmonic Suppression and Bandwidth Enhancement
- Study on Glass-Epoxy-Based Low-Cost and Compact Tip-Truncated Triangular Printed Antenna
- Design of Multilevel Sequential Rotation Feeding Networks Used for Circularly Polarized Microstrip Antenna Arrays

(14) - STEP/Course material in softcopy



Lecture_Notes_Antenna_and_Wave_Propagati.rar



AWP PPT-1.rar



ACADEMIC PLANNER

FOR THE

ACADEMIC YEAR 2024-2025

COURSE: III YEAR B. TECH -I- SEM

Subject: Data Communications & Networks

CREDITS: 4

Presented by

B. Papachary, Assoc.Prof,

Dept.of ECE

ACADEMIC PLANNER

Subject: Data Communications and Networks

S.NO

CONTENT

- (1) - **Preamble/Introduction**
- (2) - **Prerequisites**
- (3) - **Objectives and Outcomes**
- (4) - **Syllabus**
1.R20-CMREC
2.GATE
3.IES
- (5) - **List of Expert Details**
(Local/National/International with Contact details/Profile link/Blogs/their research Contribution towards the subject)
- (6) - **Journals with min 5 ref paper for literature study**
- (7) - **-Subject -Lesson plan**
- (8) - **-Suggested Books (prescribed and References)**
- (9) - **-Websites for self learning Resources like**
www.schools.com, Coursera Udemy, NPTEL etc along Registration procedures
-Question Banks 1. JNTUH/Model papers
2.GATE/IES
- (11) - **Two case study presentations with Project / Product/ Model /prototypes/ Industrial applications.**
- (12) - **Assignment Question/Innovative Assignments sets.**
- (13) - **List of topics for students Seminars with Guidelines**
- (14) - **STEP/Course material in softcopy**
- (15) - **Expert Lectures with topics & Schedules (if any)**

1. INTRODUCTION TO DATA COMMUNICATIONS AND NETWORKING:

- 1 Standards Organizations for Data Communications
- 2 Layered Network Architecture
- 3 Open Systems Interconnection (OSI)
- 4 Data Communications Circuits
- 5 Serial and parallel Data Transmission
- 6 Data communications Circuit Arrangements
- 7 Data communications Networks
- 8 Alternate Protocol Suites.

2. PREREQUISITES:

Digital Communications

3. COURSE OBJECTIVES :

1. To introduce the fundamentals of data communication networks
2. To demonstrate the functions of various protocols of the Data link layer.
3. To demonstrate the functioning of various Routing protocols.
4. To introduce the functions of various Transport layer protocols.
5. To understand the significance of application layer protocols

COURSE OUTCOMES:

Upon completing this course, the student will be able to

CO 1: Know the Categories and functions of various Data communication Networks

CO 2: Design and analyze various error detection techniques.

CO 3: Demonstrate the mechanism of routing the data in the network layer

CO 4: Know the significance of various Flow control and Congestion Control Mechanisms

CO 5: Know the Functioning of various Application layer Protocols.

4) SYLLABUS:



R22 B.Tech. ECE Syllabus

III YEAR B.TECH ECE-I SEM

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3 1/0/- 4

Data Communications & Networks

UNIT - I: Introduction to Data Communications: Components, Data Representation, Data Flow, Networks- Distributed Processing, Network Criteria, Physical Structures, Network Models, Categories of Networks Interconnection of Networks, The Internet - A Brief History, The Internet Today, Protocol and Standards - Protocols, Standards, Standards Organizations, Internet

Standards. Network Models, Layered Tasks, OSI model, Layers in OSI model, TCP/IP Protocol

Suite, Addressing Introduction, Wireless Links and Network Characteristics, WiFi: 802.11
Wireless LANs -The 802.11 Architecture,

Objective:

- Introduction to Data communication
- Different types of Network models, Interconnection of Networks
- Internet protocol, standards, and organizations
- OSI model
- TCP/IP model

UNIT - II: Data Link Layer: Links, Access Networks, and LANs- Introduction to the Link Layer, The Services Provided by the Link Layer, Types of errors, Redundancy, Detection vs Correction, Forward error correction Versus Retransmission Error-Detection and Correction Techniques, Parity Checks, Check summing Methods, Cyclic Redundancy Check (CRC) , Framing, Flow Control and Error Control protocols , Noisy less Channels and Noisy Channels, HDLC, Multiple Access Protocols, Random Access ,ALOHA, Controlled access, Channelization Protocols.

802.11 MAC Protocol, IEEE 802.11 Frames

Objective:

- Introduction to Link layer
- Types of Errors and Redundancy
- Error correction and Detection
- Parity check, Cyclic Redundancy Check (CRC)
- Flow control and Error control protocols
- HDLC
- Random access, ALOHA
- MAC protocols

UNIT - III: The Network Layer: Introduction, Forwarding and Routing, Network Service Models, Virtual Circuit and Datagram Networks-Virtual-Circuit Networks, Datagram Networks, Origins of VC and Datagram Networks, Inside a Router-Input Processing, Switching, Output Processing, Queuing, The Routing Control Plane, The Internet Protocol (IP): Forwarding and Addressing in the Internet- Datagram format, Ipv4 Addressing, Internet Control Message Protocol(ICMP), Ipv6

Objective

- Forwarding and Routing
- Virtual circuit and datagram Networks
- Concept of Router
- Queuing
- Internet protocol (IP)
- Ipv4
- Ipv6
- ICMP

UNIT - IV: Transport Layer: Introduction and Transport Layer Services : Relationship Between Transport and Network Layers, Overview of the Transport Layer in the Internet, Multiplexing and Demultiplexing, Connectionless Transport: UDP -UDP Segment Structure, UDP Checksum, Principles of Reliable Data Transfer-Building a Reliable Data Transfer Protocol, Pipelined Reliable Data Transfer Protocols, GoBack-N(GBN), Selective Repeat(SR), Connection Oriented Transport: TCP - The TCP Connection, TCP Segment Structure, Round-Trip Time Estimation and Timeout, Reliable Data Transfer, Flow Control, TCP Connection Management, Principles of Congestion Control - The Cause and the Costs of Congestion, Approaches to Congestion Control

Objective:

- Relationship Between Transport and Network Layer
- Multiplexing and Demultiplexing,
- UDP
- Reliable Data Transfer Protocol
- Go Back-N(GBN)
- Selective Repeat (SR)
- TCP
- Principles of Congestion Control

UNIT - V: Application Layer: Principles of Networking Applications – Network Application Architectures, Processes Communicating, Transport Services Available to Applications, Transport Services Provided by the File Transfer: FTP,- FTP Commands and Replies, Electronic Mail in the Internet- STMP, Comparison with HTTP, DNS-The Internet's Directory Service – Service Provided by DNS, Overview of How DNS Works, DNS Records and messages

Objective:

- Principles of Networking Applications
- FTP
- Electronic Mail in the Internet
- STMP
- HTTP
- DNS

TEXTBOOKS:

1. Computer Networking A Top-Down Approach – Kurose James F, Keith W, 6th Edition, Pearson.
2. Data Communications and Networking Behrouz A. Forouzan 4th Edition McGraw-Hill Education

REFERENCES:

1. Data communication and Networks - Bhusan Trivedi, Oxford university press, 2016
2. Computer Networks -- Andrew S Tanenbaum, 4th Edition, Pearson Education
3. Understanding Communications and Networks, 3rd Edition, W. A. Shay, Cengage Learning.

SYLLABUS – GATE:

Concept of layering: OSI and TCP/IP Protocol Stacks;

Basics of packet, circuit and virtual circuit-switching;

Data link layer: framing, error detection, Medium Access Control, Ethernet bridging;

Routing protocols: shortest path, flooding, distance vector and link state routing;

Fragmentation and IP addressing, IPv4, CIDR notation, Basics of IP support protocols (ARP, DHCP, ICMP), Network Address Translation (NAT);

Transport layer: flow control and congestion control, UDP, TCP, sockets;

Application layer protocols: DNS, SMTP, HTTP, FTP, Email.

SYLLABUS – IES:

Data link layer: framing, error detection, Medium Access Control, Ethernet bridging;

Routing protocols: shortest path, flooding, distance vector and link state routing;

Fragmentation and IP addressing, IPv4, CIDR notation, Basics of IP support protocols (ARP, DHCP, ICMP), Network Address Translation (NAT);

Transport layer: flow control and congestion control, UDP, TCP, sockets;

Application layer protocols: DNS, SMTP, HTTP, FTP, Email.

5. SUJECT EXPERTS DETAILS:

REGIONAL:

1. Dr N.S Murthy (NIT WARANGAL), Professor, Electronics & Com. Engg. Department
National Institute of Technology, Warangal - 506004, A.P, INDIA

E-Mail: nsm@nitw.ac.in

Phone No: 0870-

2462404

2. Dr.Kakarla Subba Rao, *Dept. of ECE, CBIT, Gandipet, Hyd-75.*

kakarlasubbarao@yahoo.co

m (H): (O): (M): 9440115130

NATIONAL:

1. Dr. Ganapati Panda (IIT BHUBANESWAR),

Professor, Contact no:+91 674 2306 205,

Mail id: gpanda@iitbbs.ac.in, ganapati.panda@gmail.com

2. Goutam Saha(IIT KHARGHPUR), Associate Professor,
Electronics & Electrical Communication Engineering
Contact no:+91 - 3222 - 283557 (IIT Phone)

Mail id: gsaha@ece.iitkgp.ernet.in,

<http://www.ecdept.iitkgp.ernet.in/index.php/home/faculty/gsaha>

INTERNATIONAL:

1. ***Behrouz Forouzan*** ,
emeritus professor of the Computer Information Systems department of DeAnza
College,
Phone: (408)864-8902
E-mail: forouzan@fhda.edu
2. **Andrew Stuart Tanenbaum**,

a Dutch-American computer scientist and professor emeritus of [computer science](#) at the [Vrije Universiteit Amsterdam](#) in the [Netherlands](#)..

www.cs.vu.nl/~ast

www.pearsonhighered.com/tanenbaum

2. Journals

IEEE Communications Surveys and Tutorials

<https://www.igi-global.com/journal/international-journal-business-data-communications/1087>

(7) . Lesson Plan

Name of the topic	Sub topics	No. of classes	Text books	Teaching Methods
UNIT I				
Introduction to Data Communications	Components, Data Representation	L1	T2,R1	M1
	Data Flow, Networks-Distributed Processing, Network Criteria, Physical Structures,	L2,L3	T2,R1	M1
	Network Models, Categories of Networks Interconnection of Networks	L4,L5	T2,R1	M1
	The Internet - A Brief History, The Internet Today, Protocol and Standards	L6,L7	T2,R1	M2:PP T
	Protocols, Standards, Standards Organizations, Internet Standards	L8,L9	T2,R1	M1
	Network Models, Layered Tasks,	L10,L11	T2,R1	M1
	OSI model, Layers in OSI model,	L12	T2,R1	M2:PP T
	TCP/IP Protocol Suite, Addressing Introduction	L13	T2,R1	M2:PP T
	Wireless Links and Network Characteristics,	L14 ,L15	T2,R1	M1
	WiFi: 802.11 Wireless LANs -	L16,L17	T2,R1	M1

	The 802.11 Architecture			
	No. of classes required: 17			
UNIT II				
Data Link Layer	Links, Access Networks	L18,L19	T1,R1,T2	M1
	LANs- Introduction to the Link Layer, The Services Provided by the Link Layer	L20,L21	T1,R1,T2	M1
	Types of errors, Redundancy, Detection vs Correction	L22	T1,R1,T2	M1
	Forward error correction Versus Retransmission Error-Detection and Correction Techniques, Parity Checks	L23,L24	T1,R1,T2	M1

	Check summing Methods, Cyclic Redundancy Check (CRC) , Framing	L25	T1,R1,T2	M2:PP T
	Flow Control and Error Control protocols	L26,L27	T1,R1,T2	M1
	Flow Control and Error Control protocols	L28,L29	T1,R1,T2	M1
	Noisy less Channels and Noisy Channels, HDLC, Multiple Access Protocols	L30,L31	T1,R1,T2	M1
	Random Access ,ALOHA, Controlled access, Channelization Protocols	L32	T1,R1,T2	M1
	802.11 MAC Protocol, IEEE 802.11 Frame	L33	T1,R1,T2	M1
	No. of classes required:16			
UNIT III				
The Network Layer	Introduction, Forwarding and Routing, Network Service Models,	L34,L35	T1,R1	M1
	Virtual Circuit and Datagram Networks- Virtual-Circuit Networks, Datagram Networks, Origins of VC and Datagram Networks	L36,L37	T1,R1	M2:PP T
	Inside a Router-Input Processing, Switching, Output Processing, Queuing, The Routing Control Plane	L38	T1,R1	M1
	The Internet Protocol(IP):Forwarding and	L39,L40	T1,R1	M1

	Addressing in the Internet-Datagram format, Ipv4 Addressing			
	Internet Control Message Protocol(ICMP), IPv6	L41	T1,R1	M1
	No. of classes required:08			
UNIT IV				
Transport Layer	Introduction and Transport Layer Services : Relationship Between Transport and Network Layers, Overview of the Transport Layer in the Internet	L42,L43,	T1,R1	M1
	Multiplexing and Demultiplexing, Connectionless Transport: UDP - UDP Segment Structure, UDP Checksum	L44,L45	T1,R1	M1
	Principles of Reliable Data	L46,L47	T1,R1	M1

	Transfer-Building a Reliable Data Transfer Protocol, Pipelined Reliable Data Transfer Protocols, GoBack-N(GBN), Selective Repeat(SR)			
	Connection Oriented Transport: TCP - The TCP Connection, TCP Segment Structure, Round- Trip Time Estimation and Timeout, Reliable Data Transfer, Flow Control, TCP Connection Management	L48, L49	T1,R1	M1
	Principles of Congestion Control - The Cause and the Costs of Congestion, Approaches to Congestion Control	L50, L51	T1,R1	M1
	No. of classes required:11			
UNIT V				
Application Layer	Principles of Networking Applications – Network Application Architectures,	L52, L53	T1,R1	M1
	Processes Communicating	L54	T1,R1	M1
	Transport Services Available to Applications,	L55	T1,R1	M1
	Transport Services Provided by the File Transfer	L56	T1,R1	M1
	FTP,- FTP Commands and Replies	L57	T1,R1	M1
	Electronic Mail in the Internet-STMP	L58	T1,R1	M2:PP T
	Comparison with HTTP	L59	T1,R1	M2:PP T
	DNS-The Internet's Directory Service	L60	T1,R1	M2:PP T

	Service Provided by DNS, Overview of How DNS Works, DNS Records and messages	L61, L62	T1,R1	M1
	No. of classes required:10			
	Total No. of Classes :54			

(8) SUGGESTED BOOKS:

TEXTBOOKS:

1. Computer Networking A Top-Down Approach – Kurose James F, Keith W, 6th Edition, Pearson.
2. Data Communications and Networking Behrouz A. Forouzan 4th Edition McGraw-Hill Education

REFERENCES:

1. Data communication and Networks - Bhusan Trivedi, Oxford university press, 2016
2. Computer Networks -- Andrew S Tanenbaum, 4th Edition, Pearson Education
3. Understanding Communications and Networks, 3rd Edition, W. A. Shay, Cengage Learning.

9. WEBSITES and URL's:

1. VIDEO LECTURES:
<https://www.youtube.com/watch?v=sG6WGvzmVaw>
2. IIT Bombay CN VIRTUAL LAB:
http://vlabs.iitb.ac.in/vlabs-dev/labs_local/computer-networks/labs/explist.php
- 3 .MIT OPEN COURSEWARE:
<https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-263j-data-communication-networks-fall-2002/lecture-notes/>
4. TEXT BOOKS: [https://eclass.teicrete.gr/modules/document/file.php/TP326/%CE%98%CE%B5%CF%89%CF%81%CE%AF%CE%B1%20\(Lectures\)/Computer_Networking_A_Top-](https://eclass.teicrete.gr/modules/document/file.php/TP326/%CE%98%CE%B5%CF%89%CF%81%CE%AF%CE%B1%20(Lectures)/Computer_Networking_A_Top-)

[Down_Approach.pdf](#)

<http://widi.lecturer.pens.ac.id/Teori/Komunikasi%20Data/Data%20Communications%20and%20%20By%20Behrouz%20A.Forouzan.pdf>

[Networking](#)

10. **Question Banks:**

R18

Code No: 135AE

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year I Semester Examinations, May/June - 2019

DATA COMMUNICATION AND NETWORKS

(Common to ECE, IT)

Time: 3 hours

Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries

10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

- List out the topologies used in networks. [2]
- b) Differentiate circuit switched networks and datagram networks. [3]
 - c) Explain flow control. [2]
 - d) Describe the differences between PPP and HDLC. [3]
 - e) Differentiate broadcasting and flooding. [2]
 - f) Define tunneling. [3]
 - g) Differentiate between TCP and UDP. [2]
 - h) Why three way handshake is used in TCP. [3]
 - i) What is the use of FTP? [2]
 - j) What is the header format of HTTP reply message? [3]

PART - B

(50 Marks)

- 2.a) Explain the ATM reference model and describe the functions performed by each layer.
 - b) What are the advantages and disadvantages of ring topology? [5+5]
- OR**
- 3.a) Elicit types of transmission media with their merits and demerits.
 - b) Describe the characteristics of layered architecture. [5+5]
- 4.a) What are the different types of error detection methods? Explain the CRC error detection technique using generator polynomial x^4+x^3+1 and data 11100011.
 - b) Explain the CSMA schemes with diagrams. [5+5]
- OR**
- 5.a) Elucidate PCF and DCF in 802.11 format.
 - b) A very heavily loaded 1 km long, 10-Mbps token ring has propagation speed of 200m/μsec. Fifty stations are uniformly spaced around the ring. Data frames are 256-bits, including 32 bits of overload. Acknowledgements are piggybacked onto the data frames and are included as spare bits within the data frames and are effectively free. The token is 8 bits. Is the effective data rate of this higher or lower than the effective data rate of a 10-Mbps CSMA/CD NETWORK? [5+5]
- 6.a) Differentiate DVR and OSPF.
 - b) How count to infinity problem is resolved in DVR. [5+5]
- 7.a) Explain ARP and RARP with examples.
 - b) What is purpose of ICMP? Explain its messages in detail. [5+5]
- 8.a) Explain the features and applications of UDP.
 - b) Elucidate congestion control in datagram subnets. [5+5]
- 9.a) Elucidate the congestion prevention policies.

- b) Explain the TCP header fields in detail. [5+5]
- 10.a) What is an Electronic mail? Explain the two scenarios of architecture of E-Mail.
 - b) Explain the architecture of WWW. Discuss client and server side functionality of this

architecture.

[5+5]

OR

11.a) What is SNMP? Briefly discuss the SNMP model components.

b) What is the use of DNS? Explain how it works?

[5+5]

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R18

Code No: 135AE

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year I Semester Examinations, November/December - 2018

DATA COMMUNICATION AND NETWORKS

(Common toECE, IT)

Time: 3 hours

Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

- | | | |
|------|---|--------------|
| 1.a) | components in a network. | List various |
| b) | List and define different network topologies. | [2] |
| c) | Define bit stuffing and character stuffing. | [3] |
| d) | Briefly discuss about ALOHA. | [2] |
| e) | Why the class C is most commonly used Network class? | [3] |
| f) | Discuss how address mapping is performed. | [2] |
| g) | Mention Congestion Prevention Policies and how does it work. | [3] |
| h) | Flow control and Error control both are properties of Transport Layer and Data Link Layer. What you think is it duplicity of properties in both layer or is it ok? Comment. | [2] |
| i) | Define SNMP protocol. | [3] |
| j) | Discuss the properties of file transfer protocol. | [2] |

PART - B

(50 Marks)

2. With a neat diagram explain the OSI reference model in detail? Explain the functions performed in each layer. [10]

OR

3. What is multiplexing? Explain in detail about various types of multiplexing. [10]

4. Describe various error detection and correction technique. The generator polynomial is x^3+x+1 . A sender want to send data 1001. Generate CRC code. Also describe error checking process if 3rd bit is inverted from the left. [10]
OR
5. What is high level data link control (HDLC)? Explain HDLC frame format in detail. [10]
6. What is classful addressing? Discuss class A, class B, class C, class D, class E address with its range in decimal dotted notation and example. [10]
OR
7. Give an example to explain any one of the multicasting routing algorithm. [10]
8. Discuss the transport layer service primitives. What do you understand by 3 way hand shake Technique? Also discuss the TCP connection management. [10]
9. Compare and contrast between integrated services and Differential Services. [10]
10. Explain name – address and address – name resolution process. [10]
OR
11. Describe the various parts of e-mail address and show the process of sending and receiving e-mails. [10]

R18

Code No: 135AE

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD

B. Tech III Year I Semester Examinations, November/December - 2018
DATA COMMUNICATION AND NETWORKS
(ECE)

- 1 Answer the following: (10 X 02 = 20 Marks)
 - (a) Differentiate simplex and duplex communication systems.
 - (b) How data is represented in case of ASCII coding system?
 - (c) Describe the functions of session and application layers.
 - (d) Describe unipolar and bipolar signal representation codes.
 - (e) If the bit rate = 3000 and each signal element carries 6 bits. Find the baud rate.
 - (f) Differentiate between wireless LAN and Bluetooth.
 - (g) State modem specifications.
 - (h) Mention the QOS parameters of network service.
 - (i) What is congestion and how it occurs?
 - (j) Explain the principle of datagram.

PART-B

(Answer all five units, 5 X 10 = 50 Marks)

- 2 (a) What are the applications and advantages of data communication networks?
(b) Explain the classification of data communication networks.

OR

- 3 (a) What are the principles used in layer architecture?
(b) What are the merits and demerits of TCP/IP model over ISO OSI model?
- 4 (a) Describe various modes of data transmission.
(b) Explain the need for flow control in the data link layer.

OR

- 5 (a) What are the advantages of burst codes and how this is achieved?
(b) Discuss about error control protocol with diagram.
- 6 What are the differences between frequency division multiple access & code division multiple access and discuss them?

OR

- 7 Classify wireless LANs & wired LANs and give LAN standards.
- 8 Explain the various methods used by TCP for congestion control.

OR

- 9 (a) Describe the distance vector routing algorithm.
(b) Discuss IP addressing procedure and its advantages.
- 10 (a) List the transport layer's quality of service parameters and explain them.
(b) Under what conditions of delay, bandwidth, load and packet loss will TCP retransmit significant volume data unnecessarily.

OR

- 11 (a) How web security can be achieved? What are the different mechanisms?
(b) Explain the operation of any one authentication protocol with a neat diagram.

12. Assignment Question :

Unit -1

1. Explain how OSI and ISO related to each other are
2. Explain ISO/OSI reference model with neat diagram?

3. Define topology and explain and explain the topologies of networks?
4. Explain the transmission modes in details?
5. Define circuit switching networks in details?.
6. Define virtual circuit networks in details?

Unit-II

- 1.State the functions of MAC?.
2. How performance is improved in CSMA/CD protocol compared to CSMA protocol? Explain?
3. How CSMA/CA differ from CSMA/CD .explain in brief?. How performance is improved in CSMA/CD.
4. Discuss the MAC layer functions of IEEE 802.11?.
4. Discuss the MAC layer functions of IEEE 802.11?.
5. Explain the frames format ,operation and ring maintenance fracture of IEEE 802.5 MAC protocol

Unit-III

- 1.Explain network layer logical addressing?.
- 2.Illustrate internetworking and tunneling?.
- 3.Explain in details of ICMP,IGMP?
- 4.Explain uni-cast routing protocols in details?.
- 5.Explain multicast routing protocols in details?.

Unit-IV

- 1.Explain in detail about process to process delivery?.
- 2.Difference between UDP and TCP protocols?.
- 3.Illustrate the congestion control in details?.
- 4.Explain quality of services in switching networks?.
- 5.Explain data traffic congestion in detail?.

Unit-V

- 1.Explain in details of domain name space?.
- 2.Explain in details of electronic mails?.
- 3.Explain in details of SMTP?.
- 4.Explain in details of WWW?.
- 5.Explain in details of SNMP?.

13) List of topics for student's seminars:

- Biometric authentication and algorithms.
- Fuzzy Systems.
- Network Security.
- Scientific and Engineering Computing.
- Applications of Computer Science in Modelling.
- Neural Networks.

➤ Cryptography.

(14) - STEP/Course material in softcopy



DCN MATREILS.rar

15 . Expert Lectures & Schedules

Si No	Lecture Name	Dept	College	Contact no	Schedule s
1	Dr T. Pothalayya	ECE	VBIT	9966933132	Aug-2023
2	Dr K Pradeep Reddy	CSE	CMRIT	9848843987	Sept-2023

CO-PO Matrix:

Course Outcomes (CO)	PO 1	PO2	PO3	PO4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2
EC603P C.1	3	3	2	2		-	-	-	-	-	3	-
EC603P C.2	3	3	3	2	-	-	-	-	-	-	3	-
EC603P C.3	3	3	3	2	-	-	-	-	-	-	3	2
EC603P C.4	3	3	3	2	-	-	-	-	-	-	3	2
EC603P C.5	3	3	2	2	-	-	-	-	-	-	3	2

Course Outcome (CO)-Program Specific Outcome (PSO) Matrix:

Course Outcomes (CO's)	PSO1	PSO2
EC603P C.1	3	3
EC603P	3	3

C.2		
EC603P C.3	3	3
EC603P C.4	3	3
EC603P C.5	3	3



ACADEMIC PLAN
FOR
ACADEMIC YEAR
2024-25

COURSE: III YEAR B.TECH ECE-II-SEM-R22

SUBJECT: Digital Signal Processing

CREDITS: 4

ACADEMIC PLANNER

Subject: Digital Signal Processing

S.NO

CONTENT

- | | | |
|------|---|---|
| (1) | - | Preamble/Introduction |
| (2) | - | Prerequisites |
| (3) | - | Objectives and Outcomes |
| (4) | - | Syllabus
1. JNTU/R20-CMREC
2. GATE
3. IES |
| (5) | - | List of Expert Details
(Local/National/International with Contact details/Profile link/Blogs/their research Contribution towards the subject) |
| (6) | - | Journals with min 5 ref paper for literature study |
| (7) | - | Subject -Lesson plan |
| (8) | - | Suggested Books (prescribed and References) |
| (9) | - | Websites for self learning Resources like
(www.geeksforgeeks.org, www.schools.com, Coursera ,edX, Udemy, Khan Academy, NPTEL etc along Registration procedures) |
| (10) | - | Question Banks
1.JNTUH/Model papers
2. GATE |
| (11) | - | Two case study presentations with Project / Product/ Model /prototypes/ Industrial applications. |
| (12) | - | Assignment Question/Innovative Assignments sets. |

- | |
|--|
| <p>(13) - List of topics for students Seminars with Guidelines</p> <p>(14) - STEP/Course material in softcopy</p> <p>(15) - Expert Lectures with topics & Schedules(if any)</p> |
|--|

(1) PREAMBLE/INTRODUCTION:

Signals analysis is very important in daily life. Hence it is required to study the different signals (continuous and discrete) and their properties. The behavior of the signals in time and frequency domain is important in analyzing the response of the network. The tools like FFT, DFT, Z- transforms may be used in the analysis of the signals. Filters must be required to eliminate the unwanted signals. Hence digital filter design also required to be studied. Sampling of signals is required to convert continuous to discrete signals. To have knowledge on the implementation signals, DSP processors must be studied.

(2) PREREQUISITES:

Signals and Systems

(3) COURSE OBJECTIVE AND OUTCOMES:

Digital signal processing is the processing of digitized discrete-time sampled signals. Processing is done by general-purpose computers or by digital circuits such as ASICs, field-programmable gate arrays or specialized digital signal processors (DSP chips). Typical arithmetical operations include fixed-point and floating-point, real-valued and complex-valued, multiplication and addition. Other typical operations supported by the hardware are circular buffers and look-up tables. Examples of algorithms are the Fast Fourier transform (FFT), finite impulse response (FIR) filter, Infinite impulse response (IIR) filter, and adaptive filters such as the Wiener and Kalman filters. The following areas covered using the digital signal Processing are

- Statistical signal processing
- Spectral estimation
- Speech signal processing
- Image processing
- Video processing
- Array processing
- Time-frequency analysis
- Filtering
- Seismic signal processing
- Data mining
- Financial signal processing

PROGRAM EDUCATION OUTCOMES

- a. Graduates will demonstrate knowledge of mathematics, science and engineering.
- b. Graduates will demonstrate an ability to identify, formulate and solve engineering problems.
- c. Graduate will demonstrate an ability to design and conduct experiments, analyze and interpret data.
- d. Graduates will demonstrate an ability to design a system, component or process as per needs and specifications.
- e. Graduates will demonstrate an ability to visualize and work on laboratory and multidisciplinary tasks.
- f. Graduate will demonstrate skills to use modern engineering tools, softwares and equipment to analyze problems.
- g. Graduates will demonstrate knowledge of professional and ethical responsibilities.
- h. Graduate will be able to communicate effectively in both verbal and written form.
- i. Graduate will show the understanding of impact of engineering solutions on the society and also will be aware of contemporary issues.
- j. Graduate will develop confidence for self education and ability for life-long learning.
- k. Graduate who can participate and succeed in competitive examinations.

PROGRAM OUTCOMES (POs)

- 1. Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems

- 2. Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- 3. Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, social, and environmental considerations.
- 4. Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- 5. Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
- 6. The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- 7. Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- 8. Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice
- 9. Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- 10. Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design

documentation, make effective presentations, and give and receive clear instructions.

11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

PROGRAM SPECIFIC OUTCOMES(PSO'S)

1. Ability to apply concepts of Electronics & Communication Engineering to associated research areas of electronics, communication, signal processing, VLSI, Embedded systems
2. Ability to design, analyze and simulate a variety of Electronics & Communication functional elements using hardware and software tools along with analytic skills

Course Name: Digital Signal Processing (EC602PC)

EC602PC.1	Understand the LTI system characteristics and Multirate signal processing.
EC602PC.2	Understand the inter-relationship between DFT and various transforms.
EC602PC.3	Design a digital IIR filter for a given specifications.
EC602PC.4	Design a digital FIR filter for a given specifications.
EC602PC.5	Understand the significance of various filter structures and effects of round off errors.
EC602PC.6	Compare the tradeoffs between normal and multi rate DSP techniques and can explore the finite

	length word effects.
	Perform time, frequency, and Z -transform analysis on signals and systems.

CO-PO Matrix:

Course Outcomes (CO)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
EC602PC.1	3	3	2	2		-	-	-	-	-	3	-
EC602PC.2	3	3	3	2	-	-	-	-	-	-	3	-
EC602PC.3	3	3	3	2	-	-	-	-	-	-	3	2
EC602PC.4	3	3	3	2	-	-	-	-	-	-	3	2
EC602PC.5	3	3	2	2	-	-	-	-	-	-	3	2
EC602PC.6	3	2	1	2	-	-	-	-	-	-	3	2

Course Outcome (CO)-Program Specific Outcome (PSO) Matrix:

Course Outcomes (CO's)	PSO1	PSO2
EC602PC.1	3	3
EC602PC.2	3	3
EC602PC.3	3	3
EC602PC.4	3	3
EC602PC.5	3	3
EC602PC.6	2	2

SCOPE:

Signal processing is an area of systems engineering, electrical engineering and applied mathematics that deals with operations on or analysis of analog as well as digitized signals, representing time-varying or spatially varying physical quantities. Signals of interest can include sound, electromagnetic radiation, images, and sensor readings, for example biological measurements such as electrocardiograms, control system signals, telecommunication transmission signals, and many others

(4) SYLLABUS:

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY

HYDERABAD

III YEAR B.TECH ECE-II SEM

L/T/P C

3/ 1/- 4

Digital Signal Processing

UNIT-I

Introduction: Introduction to DSP, Discrete time signals & Sequences, conversion of continuous to discrete signal, Normalized frequency, Linear shift invariant systems, stability, Causality, Linear constant coefficient difference equations, Frequency domain representation of discrete time signals and systems.

Multi rate digital signal processing: Multi rate digital signal processing introduction, Down sampling, decimation, Up sampling, interpolation, Sampling rate conversion.

UNIT-II

Discrete Fourier series: Fourier Series, Fourier Transform, Laplace Transform and Z-Transform relation, DFS Representation of Periodic Sequences, Properties of Discrete Fourier Series, Discrete Fourier Transforms: Properties of DFT, Linear Convolution of Sequences using DFT, Computation of DFT: Over-Lap Add Method, Over-Lap Save Method, Relation between DTFT, DFS, DFT and Z Transform.

Fast Fourier Transforms: Fast Fourier Transforms (FFT), Radix-2 DIT FFT, DIF FFT, Inverse FFT, FFT with general radix-N

UNIT-III

IIR digital filters: Analog filter approximations-Butterworth, chebychev, Design of IIR digital filters from Analog filters, Step & Impulse invariant method, Bilinear transformation method, Spectral transformations

UNIT-IV

FIR digital filters: Characteristics of FIR digital filters, frequency response, Design of FIR filters using Fourier method, Digital filters using Window techniques, Frequency Sampling technique, Comparison of IIR & FIR filters

UNIT-V:

Realization of digital filters: Application of Z-transforms, Solution of difference equations of digital filters, System function, Stability criterion, Frequency response of stable systems, Realization of digital filters-Direct, canonic, cascade and parallel forms

Finite word length effects: Finite word length effects, Limit cycles, over flow oscillations, round off noise in IIR digital filters, Computational output round off noise, methods to prevent over flow, Trade off between round off and overflow noise, Measurement of coefficient quantization effects through pole-zero movement, Dead band effects.

TEXT BOOKS:

1. Discrete Time Signal Processing – A. V. Oppenheim and R.W. Schaffer, PHI, 2009
2. Digital Signal Processing, Principles, Algorithms, and Applications: John G. Proakis, Dimitris G. Manolakis, Pearson Education / PHI, 2007.

REFERENCES:

1. Digital Signal Processing – Fundamentals and Applications – Li Tan, Elsevier, 2008
2. Fundamentals of Digital Signal Processing using MATLAB – Robert J. Schilling, Sandra L. Harris, Thomson, 2007
3. Digital Signal Processing – S. Salivahanan, A. Vallavaraj and C. Gnanapriya, TMH, 2009
4. Digital Signal Processing - A Practical approach, Emmanuel C. Ifeakor and Barrie W. Jervis, 2nd Edition, Pearson Education, 2009

GATE SYLLABUS:**Electronics and Communications Engineering: Signals and Systems**

Continuous-time signals: Fourier series and Fourier transform representations, sampling theorem and applications; Discrete-time signals: discrete-time Fourier transform (DTFT), DFT, FFT, Z-transform, interpolation of discrete-time signals; LTI systems: definition and properties, causality, stability, impulse response, convolution, poles and zeros, parallel and cascade structure, frequency response, group delay, phase delay, digital filter design techniques.

IES SYLLABUS:**Electronics and Tele Communications Engineering: Systems and Signal Processing**

Systems and Signal Processing : Representation of continuous and discrete-time signals, shifting and scaling operations, linear, time-invariant and causal systems, Fourier series representation of continuous periodic signals, sampling theorem, Fourier and Laplace transform, Z transforms, Discrete Fourier, transform, FFT, linear convolution, discrete cosine transform, FIR filter, IIR filter, bilinear transformation.

(5) SUBJECT EXPERTS DETAILS:**REGIONAL:**

1. Dr. Nukala Suryanarayana Murthy B.E.,M.S.,Ph.D
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Simula Research Laboratory, Norway

Contact Number:+47 465 65 641

[Url:https://scholar.google.com/citations?user=8H5s9vEAAAAJ&hl=en](https://scholar.google.com/citations?user=8H5s9vEAAAAJ&hl=en)

(6) JOURNAL WITH MIN 5 REF PAPERS FOR LITERATURE SURVEY STUDY:

1. <https://ieeexplore.ieee.org/document/1614066/authors#authors>

Title: Compressed sensing

2. <https://ieeexplore.ieee.org/document/482137>

Title: Splitting the unit delay [FIR/all pass filters design]

3. <https://ieeexplore.ieee.org/document/109205>

Title: Frequency-domain and multirate adaptive filtering

4. <https://ieeexplore.ieee.org/document/1161901>

Title: The use of fast Fourier transform for the estimation of power spectra: A method based on time averaging over short, modified periodograms.

5. <https://ieeexplore.ieee.org/document/1162619>

Title: A new hardware realization of digital filters

(7) Lesson Plan

Name of the topic	Sub topics	No. of classes	Text books	Remarks
UNIT I				
Introduction	Introduction to DSP	L1	T1,R1	1
	Discrete time signals & Sequences, conversion of continuous to discrete signal,	L2,L3	T1,R1	1
	Normalized frequency, Linear shift invariant systems, stability	L4,L5	T1,R1	1
	Causality, Linear constant coefficient difference equations	L6,L7	T1,R1	1
	Frequency domain representation of discrete time signals and systems	L8,L9	T1,R1	2
	Multi rate digital signal processing introduction	L10	T1,R1	1
	Down sampling, decimation	L11	T1,R1	1
	Up sampling, interpolation	L12	T1,R1	1
	Sampling rate conversion	L13	T1,R1	1
	Conversion of band pass signals	L14	T1,R1	1
	concept of resampling	L15	T1,R1	1
	Applications of multi rate signal	L16	T1,R1	1

	processing			
No. of classes required				12
UNIT II				
Discrete Fourier Series	DFS representation, Properties	L17,L18	T1,R1,T2	2
	DFT, Properties	L19,L20	T1,R1,T2	2
	Linear Convolution of sequences using DFT	L21	T1,R1,T2	1
	Overlap add method, Overlap save method	L22,L23	T1,R1,T2	2
	Relation between DTFT,DFS,DFT and Z-Transform	L24	T1,R1,T2	1
Fast Fourier Transforms	Fast Fourier Transforms(FFT)	L25,L26	T1,R1,T2	1
	Radix-2 DIT FFT	L27,L28	T1,R1,T2	1
	DIF FFT	L29,L30	T1,R1,T2	1
	Inverse FFT	L31	T1,R1,T2	1
	FFT with general radix-N	L32	T1,R1,T2	1
No. of classes required				12
UNIT III				
IIR digital filters	Analog filter approximations- Butterworth, chebychev	L33,L34	T1,R1	2
	Design of IIR digital filters from analog filters	L35,L36	T1,R1	2
	Step & Impulse invariant method	L37	T1,R1	1
	Bilinear transformation method	L38,L39	T1,R1	2
	Spectral transformations	L40	T1,R1	1
	No. of classes required			8
UNIT IV				
	Characteristics of FIR digital filters,	L41,L42	T1,R1	2

FIR digital filters	frequency response			
	Design of FIR filters using Fourier method	L43,L44	T1,R1	1
	Digital filters using Window techniques	L45,L46	T1,R1	2
	Frequency Sampling technique	L47	T1,R1	1
	Comparison of IIR & FIR filters	L48	T1,R1	1
No. of classes required				8
UNIT V				
Realization of digital filters	Application of Z-transforms	L49,L50	T1,R1	2
	Solution of difference equations of digital filters	L51	T1,R1	1
	System function, Stability criterion	L52	T1,R1	1
	Frequency response of stable systems	L53 ,L54	T1,R1	1
	Realization of digital filters-Direct, canonic, cascade and parallel forms	L55,L56	T1,R1	2
Finite word length effects	Finite word length effects	L57	T1,R1	1
	Limit cycles, over flow oscillations, round off noise in IIR digital filters	L58	T1,R1	1
	Computational output round off noise, methods to prevent over flow	L59	T1,R1	1
	Trade off between round off and overflow noise	L60	T1,R1	1
	Measurement of coefficient quantization effects through pole-zero movement	L61	T1,R1	1
	Dead band effects	L62	T1,R1	1
No. of classes required				12
Total No. of Classes				52

(8) SUGGESTED BOOKS:

TEXT BOOKS:

T1:-Digital signal processing, principles, algorithms and applications: Johnn G.Proakis, Dimitris G.Monalakis, Pearson Education/PHI 2007

T2:-Discrete Time Signal Processing –A.V.Oppenheim and R.W.Schaffer,PHI 2009

T 3:-Fundamentals of Digital Signal Processing-Loney Ludeman, John Wiley, 2009

REFERENCES:

R1:-Digital Signal Processing –S.Salivahanan,A.Vallavaraj and C.Gnana Priya,TMH ,2009

R2:-Discrete Time Signal Processing-Fundamentals and Applications-Litan, Elsevier,2008

R3:-Fundamentals of Discrete Time Signal Processing using Matlab- Robertj.Schilling,Sandra L.Harris,Thomson ,2007

R4:-Digital signal processing a practical approach by Emmanuel C. Ifeachor

(9) WEBSITES FOR SELF LEARNING RESOURCES:

1. NPTEL VIDEO LECTURES:

<https://nptel.ac.in/courses/117/102/117102060/>

2. COURSERA:

<https://www.coursera.org/specializations/digital-signal-processing#howItWorks>

3. MIT OPEN COURSEWARE:

<http://ocw.mit.edu/resources/res-6-008-digital-signal-processing-spring-2011/>

4. EDX:

<https://www.edx.org/course/discrete-time-signal-processing-4>

4. UDEMY:

<https://www.udemy.com/course/signal-processing-dft-fft/>

(10) QUESTION BANK:



QUESTION BANK-JNTUH-MODEL.rar

(11) CASE STUDY

Project 1:-

TITLE:-A Comparative Study of ECG Beats Variability Classification Based on Different Machine Learning Algorithms

Abstract:-

The electrocardiogram (ECG) signal is a method that uses electrodes to record cardiac rates along with sensing minute electrical fluctuations for each cardiac rate. The information is utilized to analyze abrupt cardiac function like arrhythmias and conduction disturbance. The paper proposes strategy classifying ECG signal using various technique. The preprocessing stage includes filtering of input signal via low pass, high pass including Butterworth filter in order to remove clamour of high frequency. From signal, the excess clamour is sliced by Butterworth filter. The peak points are detected by peak detection algorithm, and the signal features are extracted using statistical parameters. At last, extracted feature classification is done via GWO-MSVM, SVM, Adaboost, ANN and Naive Bayes classifier to classify the ECG signal database into normal or abnormal ECG signal. The experimental result indicates the precision of the GWO-MSVM, SVM, Adaboost, ANN and Naive Bayes classifier is 99.9%, 94%, 93%,87.57% and 85.28%. When compared with other classifier, it was determined that precision of GWO-MSVM classifier is high.

Project 2:-

TITLE:- Monophonic Pitch Recognition

Abstract:-

The purpose of this project is to create a system that automatically converts monophonic music into its MIDI equivalent. Automatic pitch recognition allows for numerous commercial applications, including automatic transcription and digital storage of live performances.

It is also desirable to be able to take an audio signal as an input and create a MIDI equivalent score because the MIDI information can be used to replace the original audio signal sounds with any sound the user would like. For example, if a piano composition is entered into the system, the resulting MIDI out could be used to trigger guitar samples.

The main deliverable for this project is a DSP evaluation board that takes a monophonic analog audio signal (ex. a recorder or someone's voice creating one pitch at a time), analyzes the signal for its fundamental frequency, and outputs MIDI data that represents the pitch and timing information contained in the audio signal all in real time.

(12) ASSIGNMENT:

Assignment1 :(From 1 unit)

PART-A:

1. a) Discuss various Discrete time sequences and mention the importance of each sequence.

b) Define an LTI system and derive the expression for the output response of an LTI system whose input sequence is $x(n)$ and impulse function of the system is $h(n)$.

2. a) Define Linearity, Time Invariant, Stable and Casual w.r.to a system.

b) Check whether the system defined by the following difference equation satisfy the conditions mentioned above $y(n) = 2x(n) - 4x(n-1) + 6x(n-2) + y(n-1)$.

3. a) Prove that the recursive system described by the linear constant coefficient difference equation described by $y(n) = ay(n-1) + x(n)$ is liner and Time invariant.

b) Determine whether the LTI recursive system described above is stable or not.

4. (a) What is Signal Processing and list the advantages, Limitations of Digital Signal Processing. List out some applications of it.

(b) Discuss in brief about the classification of signals.

5. (a) Give the differences between analog and digital system.

(b) Give the block diagram of Analog Signal Processing and compare with Digital signal Processing system and list out the applications of each.

6. (a) Define the operations of a signal - Time scaling, Amplitude Scaling and folding.

(b) What is an LTI system? Show that an LTI system combined with time scaling property may result in an Time-variant system.

PART-B:

1. a) Define transfer function of Digital System in general, and the relation of it with input/output difference equation.

b) Obtain the cascade structure of 1st order canonic form of the following system.
 $y(n) - 3y(n-1) - 4y(n-2) = x(n) + 2x(n-1)$

2. a) Discuss about cascade and parallel form realization structures of IIR systems.

b) Obtain the parallel and cascade realization structures for the system function given by $H(Z) = (1+0.5Z^{-1}) / [(1+0.5Z^{-1})(1+0.5Z^{-1}+0.25Z^{-2})]$.

3. a) Define System function and bring out its relationship with difference equation

b) Determine the system function and also find its poles and zeros if $y(n)+3y(n-1)+1/8y(n-2) = x(n)+x(n-1)$.

4. Obtain all the possible realization structures of the following transfer function.

$$H(Z) = 1 - b\cos_{-Z} = (1 + aZ^{-1})(1 - 2b\cos_{-Z} + b^2Z^{-2}):$$

5.a) Discuss Cascade and Parallel form realization structures of IIR systems.

b) Obtain the parallel and cascade realization structures for the system function given by $H(Z) = (1+\frac{1}{4}Z^{-1}) / (1+\frac{1}{2}Z^{-1})(1+\frac{1}{2}Z^{-1}+\frac{1}{4}Z^{-2})$.

6. (a) Determine the impulse response $h(n)$ for the system described by the second order difference equation

$$y(n)-4y(n-1)+4y(n-2) = x(n-1).$$

(b) An LTI system is described by the equation $y(n) = x(n)+0.8x(n-1)+0.7x(n-2)- 0.45y(n-2)$. Determine the transfer function of the system. Sketch its poles and zeros on the Z-plane.

7. (a) Define Phase delay and group delay.

(b) The following transfer function characterizes an FIR filter ($M=11$). Determine the magnitude response and show that the phase and group delays are constant.

8. (a) Define Z- Transform. State any four properties of Z- transform.

(b) A system has an impulse response $h(n) = \{1,2,3\}$ and output response $y(n)= \{1, 1, 2,-1, 3\}$. Determine the input sequence.

Assignment2 :(From 2 unit)

PART-A:

1. a) Explain the Frequency response of discrete systems and hence the importance of it.
b) Define DFT and obtain the relation between z- transform and DFS
- 2.a) Define DFT and IDFT.
b) Compute 8-point DFT of given sequence $x(n) = \{1,1,1,1,0,0,0,0\}$ and also compute IDFT for the result obtained with DFT and verify whether the original sequence is obtained or not.
3. a) Discuss the computational complexity of computing N-Point DFT.
b) Perform Linear convolution of the two given sequences $x(n) = \{3,1,3\}$ and $h(n) = \{2,1\}$ using DFT and IDFT.
4. (a) Determine the relationship between DFT and Fourier transform of an aperiodic sequence.

(b) Perform Linear convolution of the two sequences $x(n) = \{1, 3, 1, -2, -3, 4,5, 6\}$ and $h(n) = \{2, -1, 1\}$ using over-lap save method and verify the result using Over-lap add method.
5. (a) Compute DFT for the given sequence $x(n) = \{1, 3, 3, 4\}$.

(b) Compute linear convolution of two given sequences $x(n) = \{1, 1, 3\}$ and $h(n) = \{2, 4\}$.
6. (a) Define DFT and IDFT. Prove Circular convolution, Circular correlation and Time reversal properties of DFT.

(b) Find the IDFT of the sequence $X(K) = \{1, 2-3j, 4, 2+3j\}$.
7. a) State the properties of DFT of a delayed sequence, Time reversed sequence, circular convolution, Circular frequency shift and circular time shift.
b) Determine the response of the system whose input $x(n)$ and impulse response $h(n)$ are given by $x(n) = \{1,2\}$ and $h(n) = \{1,2\}$ using DFT and IDFT.

PART-B:

1. a) What is FFT? Explain the advantages of FFT over DFT. Obtain the signal flow graph of FFT algorithm and explain its operation.
b) Obtain the DFT of sequence $x(n) : [1,2,3,4,4,3,2,1]$ using FFT algorithm.
2. a) Compare the computational complexity of DFT and FFT.
b) An 8 point sequence is given by $x(n) = \{1,2,1,2,1,2,1,2\}$. Compute 8 point DFT of $x(n)$ using Radix-2 decimation in time FFT
3. a) What is bit reversed technique and explain it with an example?
b) What is DIT algorithm? Give the mathematical analysis of DIT algorithm using Radix-2 In-place algorithm

- 4.a) What is In-place algorithm and what is the advantage of this algorithm?
- b) Compute 8-point DFT of the given sequence $x(n) = \{1, 2, 1, 2, 1, 2, 1, 2\}$ using DIF FFT algorithm.
5. What is DIF algorithm? Give the mathematical analysis of DIF algorithm using Radix-2 In-place algorithm.
6. (a) Compare DIT and DIF FFT algorithms.
- (b) Develop the signal flow graph in computing 16-point FFT using DIT-FFT algorithm.
7. (a) Give the Basic butterfly structures of computing DFT using DIT and DIF algorithm.
- (b) Compute the IFFT for the sequence $X(K) = \{0, 1, 2, 3, 0, 0, 0, 0\}$, using DIT algorithm.
8. Develop a radix -2 DIF / FFT algorithm for evaluating the DFT for $N=8$ and hence determine the 8-point DFT of the sequence $x(n) = \{0, 1, 0, 1, 0, 1, 0, 1\}$.

Assignment3 :(From 3 unit)

PART-A

1. a) Explain clearly about the design of IIR filters from analog prototypes and hence bring out the constraints.
- b) Design a digital Low pass filter, with following specifications. Using Butterworth approximation and Bilinear Transformation.
 Pass band ripple ≤ 1 dB; Pass band edge = 4 kHz,
 Stop band $A_{Hn} \geq 40$ dB; Stop band edge = 6 kHz
 Sampling rate = 24 kHz. Assume suitable data.
2. a) Explain how aliasing effect occurs in designing of IIR filters using impulse invariant technique.
- b) Compute the poles of an analog Butterworth filter transfer function that satisfies the constraints
 $0.707 \leq |H(j\Omega)| \leq 1 ; 0 \leq \Omega \leq 2$
 $|H(j\Omega)| \leq 0.1 ; \Omega \geq 4$ and determine $H_a(s)$ and hence obtain $H(z)$ using Bilinear transformation.
3. a) Compare Impulse invariant and Bilinear transformation techniques.
- b) Discuss the procedure of converting an IIR analog filter into digital filter using bilinear transformation. List out its merits and demerits.
4. (a) In a speech recording system with a sampling frequency of 10,000 Hz, the speech is corrupted by random noise. To remove the random noise while preserving speech information, the following specifications are given.
 Speech frequency range : 0 - 3000 KHz.
 Stop band range : 4,000 - 5,000 KHz.

Passband ripple : 3 dB

Stopband attenuation : 25 dB.

Determine the filter order and transfer function using butterworth IIR filter.

(b) How Chebyshev filter approximation is superior than butterworth filter approximation.

5. (a) What is Bilinear transformation and sketch the mapping of S-plane into Z-plane in bilinear transformation.

(b) Discuss the problems encountered in design of digital filter using Impulse invariant and bilinear transformation techniques.

6. (a) Compare Butterworth and Chebyshev approximation techniques of filter designing.

(b) Design a Digital Butterworth LPF using Bilinear transformation technique for the following specifications

$$0.707 \leq |H(e^{j\omega})| \leq 1; 0 \leq \omega \leq 0.2 \text{ rad/s} \\ |H(e^{j\omega})| \leq 0.08; 0.4 \leq \omega \leq \pi$$

7. (a) Discuss in detail the procedure of designing an analog filter using Butterworth approximation technique.

(b) Explain how to convert an analog filter transfer function into digital filter transfer function using Bilinear transformation.

Assignment4 :(From 4 unit)

1. a) Discuss about the importance of windowing technique in the design of FIR filters and compare Barlett and Hamming windows w.r.t. Rectangular windows.

b) What is linear phase? What is the condition for linear phase systems in FIR systems? Explain.

2. Design an FIR Digital high pass filter using Rectangular window whose cut off frequency is 3 rad/s and length of window N=9. Draw and comment on magnitude response characteristics of w.r.t side lobe levels and main lobe width. Realize the same using direct form structure.

3.a) Define an IIR filter and bring out the constraints to be maintained in conversion of an analog filter into digital filter.

b) Discuss the procedure of converting an IIR analog filter into digital filter using impulse invariant transformation.

4.a) Explain briefly the frequency response of LTI systems.

b) Determine the frequency response of the second order system given by the difference equation

$$y(n) = 2r \cos \omega_0 y(n-1) - r^2 y(n-2) + x(n) - r \cos \omega_0 x(n-1).$$

5.(a) What are the desirable characteristics of windowing function to be satisfied in filter design.

(b) Design an FIR Digital Low pass filter using Blackman-Tukey window whose cutoff freq is 1.2 rad/s and length of window $N=5$.

6. (a) FIR filters are always stable and have linear phase characteristics. Justify.

(b) Design an FIR Digital Band stop filter using rectangular window whose upper and lower cut off frequencies are 4 & 5 rad/s and length of window $N=9$. Realize the filter using linear phase Realization structure.

7. (a) Compare FIR and IIR filters.

(b) Justify the statement that FIR filters can have linear phase characteristics.

8. (a) Convert the single pole low pass Butterworth filter with system function $H(Z) = 0.245(1 + Z^{-1}) / (1 - 0.509 Z^{-1})$ into a band pass filter with upper and lower cut off frequencies ω_u and ω_l . The low pass filter has 3dB band width $\omega_p = 0.2$.

(b) State advantages of IIR filters over FIR filters.

Assignment5 :(From 5 unit)

PART- A:

1. a) What is Multirate processing? Discuss the necessity for it.

b) Explain in detail about the Implementation of interpolation & decimation processes and hence discuss about optimum filter requirements.

2.a) Explain the necessity of Multirate signal processing and hence define Decimation and Interpolation.

b) Discuss the sampling rate conversion by a factor I/D .

3.a) What are Multirate Systems? Discuss their importance in real time processing of signals.

b) Explain the process of Interpolation by a factor- I and also discuss how the images are eliminated with a neat block diagram.

4.a) Discuss the various cases of frequency responses of FIR filters.

b) Compare various windowing techniques in FIR filter design w.r.t beam width and side lobes.

5. (a) Discuss the process of Decimation by a factor D and hence explain how the aliasing effect can be avoided.

(b) Explain the process of performing subband coding for speech signals. [7+8]

6. (a) Design a poly phase filter structure for a sequence $x(n) = \{x(0), x(1), x(2), x(3)\}$ interpolated by a factor 3 and consider the filter length $N=9$. (b) Explain the process of performing subband coding for speech signals.

7. (a) Discuss the process of Decimation by a factor D with a neat block diagram.

(b) Plot the signals and their corresponding spectra for rational sampling rate conversion by a) $I/D = 5/3$ and

b) $I/D = 3/5$. Assume that the spectra of input signal $x(n)$ occupies the entire range $-\pi$ to π .

PART-B:

1. (a) Discuss the effects due to finite word length in Direct form - I and II structures.

(b) Discuss the effect of quantization of coefficients in FIR filters.

2. (a) Discuss finite word length effects of implementation of FFT algorithm.

(b) What is scaling? Discuss how to reduce finite word length effects using scaling.

3. (a) Discuss the effect of ADC Quantization noise on Signal Quality.

(b) Discuss finite word length effects of implementation of FFT algorithm.

4. What are Limit Cycles? Discuss various types of Limit Cycles in brief.

SLIP TESTS:

Slip tests are conducted in the class rooms.

8 slip tests are conducted per course.

3 questions are given for each slip test.

Instructions:

Slip test should be in written documents with the following requirements.

1) Cover page with name, roll number, course name and course section.

2) A page with questions. 3) Solutions/Explanations.

Slip Test1 :(From unit 1)

1. a) Discuss various Discrete time sequences and mention the importance of each sequence.

b) Define an LTI system and derive the expression for the output response of an LTI system whose input sequence is $x(n)$ and impulse function of the system is $h(n)$.

2. a) Define Linearity, Time Invariant, Stable and Casual w.r.to a system.

- b) Check whether the system defined by the following difference equation satisfy the conditions mentioned above $y(n) = 2x(n) - 4x(n-1) + 6x(n-2) + y(n-1)$.
3. a) Prove that the recursive system described by the linear constant coefficient difference equation described by $y(n) = ay(n-1) + x(n)$ is linear and Time invariant.
- b) Determine whether the LTI recursive system described above is stable or not.
4. a) Discuss Cascade and Parallel form realization structures of IIR systems.
- b) Obtain the parallel and cascade realization structures for the system function given by $H(Z) = (1 + \frac{1}{4}Z^{-1}) / (1 + \frac{1}{2}Z^{-1})(1 + \frac{1}{2}Z^{-1} + \frac{1}{4}Z^{-2})$.
5. (a) Determine the impulse response $h(n)$ for the system described by the second order difference equation $y(n) - 4y(n-1) + 4y(n-2) = x(n-1)$.
- (b) An LTI system is described by the equation $y(n) = x(n) + 0.8x(n-1) + 0.7x(n-2) - 0.45y(n-2)$. Determine the transfer function of the system. Sketch its poles and zeros on the Z-plane.
6. a) Define System function and bring out its relationship with difference equation
- b) Determine the system function and also find its poles and zeros if $y(n) + 3y(n-1) + \frac{1}{8}y(n-2) = x(n) + x(n-1)$.

Slip Test2 :(From unit 2)

- 1.a) Define DFT and IDFT.
- b) Compute 8-point DFT of given sequence $x(n) = \{1, 2, 3, 4, 4, 3, 2, 1\}$ and also compute IDFT for the result obtained with DFT and verify whether the original sequence is obtained or not.
2. a) Discuss the computational complexity of computing N-Point DFT.
- b) Perform Linear convolution of the two given sequences $x(n) = \{1, 2, 3\}$ and $h(n) = \{2, 1\}$ using DFT and IDFT.
3. (a) Determine the relationship between DFT and Fourier transform of an aperiodic sequence.
- (b) Perform Linear convolution of the two sequences $x(n) = \{12, 3, -1, -2, -3, 4, 5, 6\}$ and $h(n) = \{2, 1, -1\}$ using over-lap save method and verify the result using Over-lap add method.
4. a) What is FFT? Explain the advantages of FFT over DFT. Obtain the signal flow graph of FFT algorithm and explain its operation.
- b) Obtain the DFT of sequence $x(n) : [1, 2, 3, 4, 4, 3, 2, 1]$ using FFT algorithm.
5. a) Compare the computational complexity of DFT and FFT.
- b) An 8 point sequence is given by $x(n) = \{1, 2, 1, 2, 1, 2, 1, 2\}$. Compute 8 point DFT of $x(n)$ using Radix-2 decimation in time FFT
6. (a) Compare DIT and DIF FFT algorithms.
- (b) Develop the signal flow graph in computing 16-point FFT using DIT-FFT algorithm.

Slip Test3 :(From unit 3)

1. a) Explain clearly about the design of IIR filters from analog prototypes and hence bring out the constraints.

b) Design a digital Low pass filter, with following specifications. Using Butterworth approximation and Bilinear Transformation.

Pass band ripple ≤ 1 dB; Pass band edge = 4 kHz,

Stop band A_{Hn} ≥ 40 dB; Stop band edge = 6 kHz

Sampling rate = 24 kHz. Assume suitable data.

2. a) Explain how aliasing effect occurs in designing of IIR filters using impulse invariant technique.

b) Compute the poles of an analog Butterworth filter transfer function that satisfies the constraints

$$0.707 \leq |H(j\Omega)| \leq 1 ; 0 \leq \Omega \leq 2$$

$|H(j\Omega)| \leq 0.1 ; \Omega \geq 4$ and determine $H_a(s)$ and hence obtain $H(z)$ using Bilinear transformation.

3. a) Compare Impulse invariant and Bilinear transformation techniques.

b) Discuss the procedure of converting an IIR analog filter into digital filter using bilinear transformation. List out its merits and demerits.

Slip Test4 :(From unit 4)

1. a) Discuss about the importance of windowing technique in the design of FIR filters and compare Barlett and Hamming windows w.r.t. Rectangular windows.

b) What is linear phase? What is the condition for linear phase systems in FIR systems? Explain.

2. Design an FIR Digital high pass filter using Rectangular window whose cut off frequency is 3 rad/s and length of window $N=9$. Draw and comment on magnitude response characteristics of w.r.t side lobe levels and main lobe width. Realize the same using direct form structure.

3.a) Define an IIR filter and bring out the constraints to be maintained in conversion of an analog filter into digital filter.

b) Discuss the procedure of converting an IIR analog filter into digital filter using impulse invariant transformation.

Slip Test 5 :(From unit 5)

1. a) What is Multirate processing? Discuss the necessity for it.

b) Explain in detail about the Implementation of interpolation & decimation processes and hence discuss about optimum filter requirements.

2.a) Explain the necessity of Multirate signal processing and hence define Decimation and Interpolation.

b) Discuss the sampling rate conversion by a factor I/D.

3. (a) Design a poly phase filter structure for a sequence $x(n) = \{x(0), x(1), x(2), x(3)\}$ interpolated by a factor 3 and consider the filter length $N=9$.

(b) Explain the process of performing subband coding for speech signals

4. (a) Discuss the effects due to finite word length in Direct form - I and II structures.

(b) Discuss the effect of quantization of coefficients in FIR filters.

5. (a) Discuss finite word length effects of implementation of FFT algorithm.

(b) What is scaling? Discuss how to reduce finite word length effects using scaling.

6. (a) Discuss the effect of ADC Quantization noise on Signal Quality.

(b) What are Limit Cycles? Discuss various types of Limit Cycles in brief

ASSESSMENT PLAN FOR ACTIONS:

Assessment plan for Assignments:

Content	Weightage
Problems	60%
Descriptive	30%
Analytical/ Reasoning	10%

Assessment plan for Slip Test:

Content	Weightage
Analyzing the problems	60%
Theoretical questions	30%
Reasoning	10%

13) List of topics for student's seminars:

- Discrete Wavelet Transform
- Audio Signal Processing
- Speech Compression And Transmission In Digital Mobile Phones
- Orthogonal Transforms For Digital Signal Processing
- Room Correction Of Sound In Hi-Fi And Sound Reinforcement Applications
- Seismic Data Processing, Analysis
- Processing Of Digital Photographs
- Complex Digital Signal Processing In Telecommunications
- A DSP Practical Application: Working On ECG Signal
- Complex Digital Filter Designs For Audio Processing In Doppler Ultrasound System
- Most Efficient Digital Filter Structures: The Potential Of Halfband Filters In Digital Signal Processing
- Applications Of Interval-Based Simulations To The Analysis And Design Of Digital LTI Systems
- Digital Camera Identification Based On Original Images.

(14) STEP/COURSE MATERIAL:



DSP-TOTAL.rar

(15) EXPERT LECTURE WITH TOPICS & SCHEDULES

S.NO	SUBJECT	TOPIC	YEAR	RESOURCE PERSON	DATE
1	DSP-I	DFS,DFT,FFT	III-II	IETE	10/05/2021
2	DSP-II	Design of FIR & IIR Filters	III-II	OTHERS	22/07/2021

ACADEMIC PLANNER

Subject: VLSI DESIGN

<u>S.NO</u>	<u>CONTENT</u>
(1) Preamble/Introduction	
(2) Prerequisites	
(3) Objectives and Outcomes	
(4) Syllabus	<ol style="list-style-type: none">1. R22-CMREC2. GATE3. IES
(5) List of Expert Details	(Local/National/International with Contact details/Profile link/Blogs/their research Contribution towards the subject)
(6) Journals with min 5 ref paper	for literature study
(7) Subject -Lesson plan	
(8) Suggested Books	(Prescribed and References)
(9) Websites for self learning Resources like	(www.geeksforgeeks.org, www.schools.com, Coursera,edX, Udemy, Khan Academy, NPTEL etc along Registration procedures)
(10) Question Banks	<ol style="list-style-type: none">1.JNTUH/Model papers2. GATE
(11) Two case study presentations with Project /	Product/ Model /prototypes/ Industrial applications.
(12) Assignment Question/Innovative Assignments sets.	
(13) List of topics for students Seminars with Guidelines	
(14) STEP/Course material in softcopy	
(15) Expert Lectures with topics &Schedules (if any)	

(1) Preamble/Introduction:

VLSI design course gives the knowledge about the fabrication of NMOS, PMOS, CMOS and their application in the present electronics world. The present course gives knowledge about different processes used for fabrication of an IC. The electrical properties of MOS transistor and analysis of CMOS, Bi-CMOS inverters is carried out. This course gives detail study on design rules, stick diagrams, logic gates, types of delays, fan-in, fan-out which effects the action of a MOS. It also gives information on data path subsystem and array subsystems, and several PLD's like PLA, PAL, CPLD and FPGA's. We also came to know about the CMOS testing principles both at system level and chip level.

(2) Prerequisites:

This subject needs the knowledge of basic semiconductor physics, concepts of MOS transistors which are covered in Electronic Devices and Circuits (EDC), digital logic fundamentals like basic gates, combinational and sequential logics in Digital System Design and Linear IC Applications.

(3) Objectives and Outcomes:

The objectives of the course are to:

1. Give exposure to different steps involved in the fabrication of ICs.
2. Explain electrical properties of MOS and Bi-CMOS devices to analyze the behavior of Inverters designed with various loads.
3. Give exposure to the design rules to be followed to draw the layout of any logic circuit.
4. Provide design concepts to design building blocks of data path of any system using gates.
5. Understand basic programmable logic devices and testing of CMOS circuits.

Course Outcomes:

Course Code. CO No	Course Outcomes (CO's)	Blooms Level's
At the end of the course student will be able to		
EC603PC.1	Explain fundamentals of IC technology and testing of CMOS circuits.	BL2
EC603PC.2	Choose an appropriate inverter using electrical properties of MOS circuits.	BL1
EC603PC.3	Develop layout of any logic circuit using concepts of stick diagrams and design rules.	BL3
EC603PC.4	Analyze characteristics of different logic gates.	BL4
EC603PC.5	Design memories and building blocks of data path of sub system.	BL6
EC603PC.6	Design logic circuits using PLA's, PAL's, FPGA's and CPLD's.	BL6

(4)-Syllabus – R22 UGC Autonomous

UNIT – I

Introduction: Introduction to IC Technology – MOS, PMOS, NMOS, CMOS and BiCMOS.

Basic Electrical Properties: Basic Electrical Properties of MOS and BiCMOS Circuits: I_{ds} - V_{ds} relationships, MOS transistor threshold Voltage, g_m , g_{ds} , Figure of merit; Pass transistor, NMOS Inverter, Various pull ups, CMOS Inverter analysis and design, Bi-CMOS Inverters.

UNIT - II

VLSI Circuit Design Processes: VLSI Design Flow, MOS Layers, Stick Diagrams, Design Rules- λ Based and Layout, Transistors Layout Diagrams for NMOS and CMOS Inverters and Gates, Scaling of MOS circuits.

UNIT – III

Gate Level Design: Logic Gates and Other complex gates, Switch logic, Alternate gate circuits, Time delays, Driving large capacitive loads, Wiring capacitance, Fan – in, Fan – out.

UNIT - IV

Data Path Subsystems: Subsystem Design, Shifters, Adders: Ripple Carry Adder, Carry Look Ahead adder, Manchester Carry Chain, Carry Skip Adder; ALUs, Multipliers: Serial Multiplier, Array Multiplier, Booth's Multiplier, Wallace Tree Multiplication; Parity generators, Comparators, Zero/One Detectors, Counters.

Array Subsystems: SRAM, DRAM, ROM, Serial Access Memories.

UNIT - V

Programmable Logic Devices: Design Approach – PLA, PAL, Standard Cells, FPGA's and CPLD's.

CMOS Testing: CMOS Testing, Test Principles, Design Strategies for test, Chip level Test Techniques.

SYLLABUS - GATE

UNIT I

Device technology: integrated circuits fabrication process, oxidation, diffusion, ion implantation, photolithography, n-tub, p-tub and twin-tub CMOS process.

UNIT II

Not applicable

UNIT III

Not applicable

UNIT IV

Not applicable

UNIT V

Not applicable

SYLLABUS - IES

UNIT I

Basics of ICs - bipolar, MOS and CMOS types.

UNIT II

Not Applicable

UNIT III

Not Applicable

UNIT IV

NMOS, PMOS and CMOS gates.

UNIT V

Not Applicable

(5) List of Expert Details (Local/National/International with Contact details/Profile link/Blogs/their research contribution towards the subject)

The Expert Details which have been mentioned below are only a few of the eminent ones known Internationally, Nationally and Locally. There are a few others known as well.

INTERNATIONAL

1. Mr. Anantha P. Chandrakasan
Professor of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
e-mail: anantha@mit.edu
2. Dr. Hanho Lee
Professor School of Information and Communication Engineering
Inha University, Korea.
e-mail: hhlee@inha.ac.kr

NATIONAL

1. Dr. Cyril Prasanna Raj P. – Professor & Dean (R&D),
M.S. Engineering College, Bangalore.
e-mail: cyril@msec.ac.in
2. Dr. Navakanta Bhat
Professor of Electrical Communication Engineering, IISC, Bangalore.
e-mail: navakant@ece.iisc.ernet.in

REGIONAL

1. Dr. J. V. R. Ravindra, Professor Dept. of ECE,
Vardhaman College of Engineering, Hyderabad.
e-mail: jvr.ravindra@vardhaman.org

(6) Journals with min 5 ref paper for literature study

INTERNATIONAL

1. ACM Transactions on Design Automation of Electronic Systems
2. IBM Journal of Research and Development
3. IEEE Transactions on CAD of Integrated Circuits and Systems
4. IEEE Transactions on Circuits and Systems Part I
5. IEEE Transactions on Circuits and Systems Part II
6. IEEE Transactions on Nanotechnology
 - i) A novel multibridge-channel MOSFET (MBCFET): fabrication technologies and

characteristics: <https://ieeexplore.ieee.org/document/1264877>

ii) A comparative study on adders: <https://ieeexplore.ieee.org/document/8300155>

7. IEEE Transactions on VLSI Systems

iii) Design and analysis of low power SRAM cells:

<https://ieeexplore.ieee.org/document/8244888>

iv) Semiconductor for 5G: <https://ieeexplore.ieee.org/document/8804702>

v) Challenges and opportunities in nano-scale VLSI design :

<https://ieeexplore.ieee.org/document/1500005>

8. Integration, The VLSI Journal (Elsevier)

9. International Journal of Electronics (Taylor & Francis Group)

10. International Journal of Modeling and Simulation (ACTA Press)

vi) Design Of A Cmos Carry Look-Ahead Adder For Self-Timed Circuits:

<https://www.tandfonline.com/doi/abs/10.1080/02286203.1997.11760338>

11. IEEE Transactions on Circuits and systems

12. IEEE Transactions on Electronic Devices.

13. The Journal of VLSI Signal Processing (Kluwer)

NATIONAL

1. Journal of the Institute of Engineers

2. Journal of the Indian Institute of Science

i) VLSI-SoC: Research Trends in VLSI and Systems on Chip :

<https://link.springer.com/book/10.1007/978-0-387-74909-9>

3. IETE Journal of Education

4. IETE Journal of Research

ii) MOS and Bipolar Memory Circuit

Techniques : <https://www.tandfonline.com/doi/abs/10.1080/03772063.1990.11436887>

iii) A Low-power and High-performance Radix-4 Multiplier Design Using a Modified Pass-transistor Logic Technique : <https://www.tandfonline.com/doi/abs/10.4103/0377-2063.81744>

5. IETE Technical Review

(7)- Subject -Lesson plan

S.NO	Topic (JNTU syllabus)	Sub-Topic	cumulative Lectures Required	Suggested Books	Remarks
		UNIT - I			

1	Introduction to IC Technology	Classification and Applications of ICs and MOSFETS	L1, L2	T1, R4	
2	MOS, PMOS, NMOS, CMOS & BiCMOS	Fabrication of PMOS, NMOS, CMOS & BiCMOS	L3, L4	T1, R4	
3	Basic Electrical Properties of MOS and Bi CMOS Circuits	Operation of NMOS and PMOS	L5	T1, R3	
4	Ids-Vds relationships	Non saturated and saturated regions	L6,L7,	T1, R3	
5	MOS transistor parameters	MOS transistor threshold Voltage V_{th} , μ_n , μ_p , figure of merit ω_0	L8,L9	T1, R3	
6	Pass transistor, NMOS Inverter	Pass transistor, NMOS Inverter	L10	T1, R3	
7	Various pull-ups	NMOS and PMOS pull-ups	L11		
8	CMOS Inverter analysis and design	I-V characteristics of CMOS Inverter	L12	T1, R3	
7	Bi-CMOS Inverters	Various Bi-CMOS Inverters	L13, L14	T1, R3	Unit I completes on L14
		UNIT – II			
8	VLSI Design Flow	VLSI Design Flow	L15	T1, R3	
9	MOS Layers	N-Diffusion, P-Diffusion, Metal, Polysilicon, Silicon dioxide	L16, L17	T1, R3	
10	Stick Diagrams	Inverter, and logic gates Stick Diagrams	L18,L19	T1, R3	
11	Design Rules and Layout	Transistor Design Rules and Layout	L20	T1, R3	
12	Layout Diagrams for NMOS and CMOS Inverters and Gates	NMOS and CMOS Inverters and Gates for Layout Diagrams	L21	T1, R2	
13	Scaling of MOS circuits, Limitations of Scaling.	Scaling factors for device parameters	L22	T1, R2	Unit II completes on L22
		UNIT-III			
14	Logic Gates and Other complex gates	AND, OR, NAND, NOR and XOR logic Gates	L23	T1, R2	
15	Switch logic, Alternative gate circuits	Switch logic using Pass transistor, Domino logic, Pseudo NMOS, Dynamic logics.	L24, L25	T1, R2	

16	Time Delays, Driving large Capacitive Loads	Estimation of CMOS Inverter delay, Driving large Capacitive Loads.	L26	T1, R2	
17	Wiring Capacitances	Inter layer and Peripheral Capacitances.	L27	T1, R2	
18	Fan-in and fan-out, Choice of layers	Effects of Fan-in and fan-out, Choice of layers	L28	T1, R2	Unit III completes on L28
		UNIT – IV			
19	Subsystem Design	Datapath, Memory, Control and I/O cells	L29, L30	T1, R2	
20	Shifters, Adders	Barrel Shifter, Ripple carry adder	L31, L32	T1, R2	
21	ALU's, Multipliers	Array and Carry save Multipliers	L33	T1, R2	
22	Parity generators, Comparators	Parity generators, Comparators	L34	T1, R2	
23	Zero/One Detectors, Counters	Asynchronous and Synchronous Counters, Zero/One Detectors,	L35	T1, R2	
24	SRAM, DRAM, ROM	SRAM Array, Synchronous DRAM, EEROM	L36, L37	T2, R2	
25	Serial Access Memories	Serial Access Memories	L38, L39	T2, R2,	Unit IV completes on L39
		UNIT – V			
27	PLA's	Architecture of PLA's	L40, L41	T2, R2	
28	FPGA's, CPLD's	Architectures FPGA's, CPLD's	L42	T2, R2	
29	Standard cells	Types of ASIC's, MPGA's,	L43, L44	T2, R2	
30	Programmable Array Logic	Architecture of PAL's	L45		
31	Programmable Array Logic	Architecture of PAL's	L46, L47	T2, R2	
32	Design Approach, Parameters influencing low power design	Design Approach, Parameters influencing low power design	L48	T2, R2	
33	Design Approach, Parameters influencing low power design	Design Approach, Parameters influencing low power design	L49	T2, R3	
34	CMOS Testing, Need for testing	Functionality and Manufacturing test	L50	T2, R1	
35	Test Principles	Fault models, Fault coverage and	L51	T2, R1	

		Simulation			
36	Design Strategies for test	DFT, Scan path	L52, L53	T2, R1	
37	System-level Test Techniques	TAP controller, BIST	L56, L57	T2, R1	
38	Chip level Test Techniques	Boundary Scan Chek, JTAG,	L54, L55	T2, R1	Unit IV completes on L57

(8) Suggested Books (prescribed and References)

TEXT BOOKS:

1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Douglas and A. Pucknell, PHI, 2005 Edition
2. CMOS VLSI Design – A Circuits and Systems Perspective, Neil H. E Weste, David Harris, Ayan Banerjee, 3rd Ed, Pearson, 2009.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. CMOS logic circuit Design - John. P. Uyemura, Springer, 2007.
3. Modern VLSI Design - Wayne Wolf, Pearson Education, 3rd Edition, 1997.
4. VLSI Design- K. Lal Kishore, V. S. V. Prabhakar, I.K International, 2009.

(9) Websites for self learning Resources like

www.geeksforgeeks.org, www.schools.com, Coursera,edx,Udemy, Khan Academy, NPTEL etc along Registration Procedures

1. https://en.wikipedia.org/wiki/Very_Large_Scale_Integration
2. <https://prezi.com/t6wpjvobwitw/very-large-scale-integration/>
3. <https://www.javatpoint.com/ic-fabrication-process>
4. <https://www.slideshare.net/varunkumar475/layout-stick-diagram-design-rules-60758496>
5. <https://www.oreilly.com/library/view/introduction-to-digital/9780470900550/chap5-sec003.html>
6. <https://in.coursera.org/learn/vlsi-cad-layout>
7. <https://in.coursera.org/learn/fpga-hardware-description-languages>
8. <https://nptel.ac.in/courses/106103016>
9. <https://www.udemy.com/course/cmos-digital-vlsi-for-beginners/>
10. https://www.researchgate.net/publication/335503256_Performance_Improvement_in_VLSI_Adders

(10) Question Bank

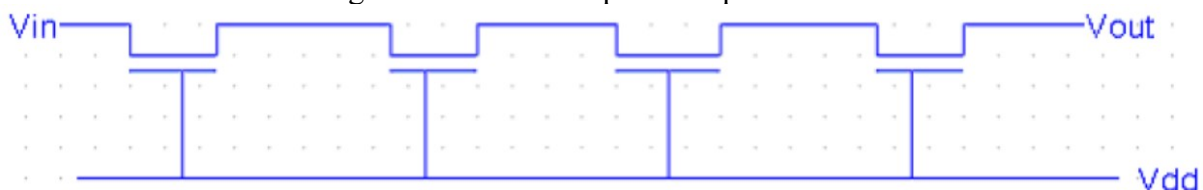
1. With neat sketches explain BICMOS fabrication process in an N well.
2. (a) With neat sketches, explain the transfer characteristic of a CMOS inverter.
(b) Derive an equation for I_{ds} of an n-channel enhancement MOSFET operating in saturation region.

3. Design a stick diagram and layout for the NMOS logic shown below

$$Y = (A + B)C.$$
4. (a) Explain clocked CMOS logic, domino logic and n-p CMOS logic.
 (b) In gate logic, compare the geometry aspects between two -input NMOS NAND and CMOS NAND gates.
5. (a) Draw the top level schematic and a floor plan for 16×16 Booth recoded multiplier and explain its operation.
 (b) Explain the tradeoffs between open, closed, and twisted bit lines in a dynamic RAM array.
6. (a) Draw and explain the Antifuse Structure for programming the PAL device.
 (b) Explain how the I/O pad is programmed in FPGA.
7. (a) Write a architecture for a 4- bit Counter in both behavioral and structural styles.
 (b) Explain with example how mixed mode simulator is more for CMOS circuits testing.
8. (a) What are the reasons of malfunctioning of chip? What are the different levels of testing?
 (b) Explain how a parallel scan is used for data path test.
 (c) What is mean by level sensitive of logic system?
9. Write in detail about integrated passive components.
10. (a) Explain various regions of CMOS inverter transfer characteristics.
 (b) For a CMOS inverter, calculate the shift in the transfer characteristic curve when β_n/β_p ratio is varied from 1/1 to 10/1.
11. (a) Write the scaling factors for different types of device parameters.
 (b) Discuss the limits due to sub threshold currents.
12. Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit.
13. (a) Draw the schematic for tiny XOR gate and explain its operation.
 (b) Draw the circuit diagram for 4-by-4 barrel shifter using complementary transmission gates and explain its shifting operation.
14. (a) Draw and explain the Antifuse Structure for programming the PAL device.
 (b) Explain how the I/O pad is programmed in FPGA.
15. (a) What type of defects are tested in manufacturing testing methods?
 (b) What is the Design for Autonomous Test and what is the basic device used in this?
 (c) What type of tests are used to check the noise margin for CMOS gates?
16. With neat sketches necessary, explain the oxidation process in the IC fabrication process.

17. (a) Draw an nMOS transistor model indicating all the components.
(b) Explain latch up problem in CMOS circuits.
18. (a) Discuss in detail the NMOS design style.
(b) Discuss CMOS design style. Compare with NMOS design style.
19. Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit.
20. (a) Explain how a Booth recoded multiplier reduces the number of adders.
(b) Draw circuit diagram of a one transistor with transistor capacitor dynamic RAM and also draw its layout.
21. (a) Draw the typical standard-cell structure showing regular-power cell and explain it.
(b) Draw and explain the pseudo-nMOS.PLA schematic for full adder and what are the advantages and disadvantages of it.
22. (a) Explain how function of system can be tested.
(b) Explain any one of the method of testing bridge faults.
(c) What type of faults can be reduced by improving layout design?
23. With neat sketches, explain in detail, all the steps involved in electron lithography process.
24. (a) Derive an equation for r_{ds} of an n channel enhancement MOSFET in linear region.
(b) Plot the transfer characteristic of an nMOS inverter as a function of V_{ds} .
25. (a) Discuss in detail the NMOS design style.
(b) Discuss CMOS design style. Compare with NMOS design style.
26. (a) Explain the requirement and operation of pass transistors and transmission gates.
(b) Compare pseudo-n MOS logic and clocked CMOS logic.
27. (a) How can the components of CMOS system design be categorized into the groups.
(b) Why is the static 6 transistor cell used for average CMOS system design?
(c) Compare the performance of CMOS Off chip and On chip memory designs.
29. (a) Draw a self timed dynamic PLA and what are the advantages of it compared to footed dynamic PLA.
(b) Explain the tradeoffs between using a transmission gate or a tristate buffer to implement an FPGA routing block.
30. (a) Explain the gate level and function level of testing.
(b) A sequential circuit with 'n' inputs and 'm' storage devices. To test this circuit how many test vectors are required?

- (c) What is sequential fault grading? Explain how it is analyzed.
31. With neat sketches explain the Ion -lithography process.
32. (a) Explain different forms of pull ups used as load, in CMOS and in enhancement & depletion modes of NMOS.
 (b) Determine the pull up to pull down ratio of an nMOS inverter driven by another nMOS transistor.
33. Design a stick diagram and layout for two input CMOS NAND gate indicating all the regions & layers.
34. Describe the following briefly
 (a) Cascaded inverters as drivers.
 (b) Super buffers.
 (c) BiCMOS drivers.
35. Explain briefly the CMOS system design based on the data path operators, memory elements, control structures and I/O cells with suitable examples.
36. (a) Draw and explain the FPGA chip architecture.
 (b) Draw and explain the AND/NOR representation of PLA.
37. (a) Explain the gate level and function level of testing.
 (b) A sequential circuit with n inputs and m storage devices. To test this circuit how many test vectors are required.
 (c) What is sequential fault grading? Explain how it is analyzed.
38. Write in detail about integrated passive components.
39. (a) Explain the operation of BiCMOS inverter? Clearly specify its characteristics.
 (b) Explain how the BiCMOS inverter performance can be improved.
40. (a) what is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.
 (b) What are the effects of scaling on V_t ?
 (c) What are design rules? Why is metal- metal spacing larger than poly – poly spacing.
41. (a) Determine an equation for the propagation delay from input to output of the pass transistor chain shown in figure 4a with the help of its equivalent circuit.



- (b) What are super Buffers?
42. (a) Explain how a Booth recoded multiplier reduces the number of adders.

(b) Draw circuit diagram of a one transistor with transistor capacitor dynamic RAM and also draw its layout.

43. (a) Draw the typical architecture of PAL and explain the operation of it.
(b) What is CPLD? Draw its basic structure and give its applications.

44. (a) What is ATPG? Explain a method of generation of test vector.
(b) Explain the terms controllability, observability and fault coverage.

45. Explain the MOS Transistor operation with the help of neat sketches in the following modes

- (a) Enhancement mode
- (b) Depletion mode

46. (a) Draw an nMOS transistor model indicating all the components.
(b) Explain latch up problem in CMOS circuits.

47. (a) What is Moore's law? Explain its relevance with respect to evolution of technology.
(b) What are different VLSI technologies available compare their speed/power performance.
(c) Why is VLSI design process presented in NMOS only?
(d) Discuss the micro electronics evolution.

48. (a) Explain clocked CMOS logic, domino logic and n-p CMOS logic.
(b) In gate logic, compare the geometry aspects between two -input NMOS NAND and CMOS NAND gates.

49. (a) Design a magnitude comparator based on the data path operators.
(b) Draw the Schematic and mask layout of array adder used in Booth Multiplier and explain the principle of multiplication in Booth Multiplier.

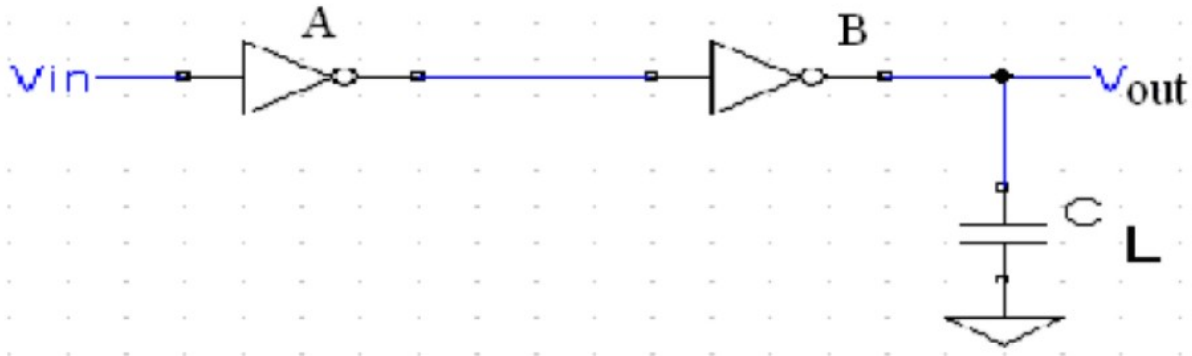
50. (a) What are the characteristics of 22V10 PAL CMOS device and draw its I/O structure.
(b) Explain any one chip architecture that used the antifuse and give its advantages.

51. (a) Draw the basic structure of parallel scan and explain how it reduces the long scan chains.
(b) Draw the state diagram of TAP Controller and explain how it provides the control signals for test data and instruction register.

52. (a) With neat sketches explain the NMOS fabrication procedure.
(b) Draw the cross sectional view of CMOS P - Well inverter.

53. (a) Derive an equation for Transconductance of an n channel enhancement MOSFET operating in active region.
(b) A PMOS transistor is operated in triode region with the following parameters.
 $V_{GS} = -4.5V$, $V_{tp} = -1V$; $V_{DS} = -2.2V$, $(W/L) = 95$, $\mu_n C_{ox} = 95 \mu A/V^2$. Find its drain current and drain source resistance.

54. (a) Discuss design rule for wires (orbit $2\mu\text{m}$ CMOS).
 (b) Discuss the transistor related design rule (orbit $2\mu\text{m}$ CMOS).
55. Two NMOS inverters are cascaded to drive a capacity load $C_L = 14C_g$ as shown in figure. Calculate the pair delay V_{in} to V_{out} in terms of τ for the given data.
- Inverter-A.
 $L_{pu} = 12\lambda$, $W_{pu} = 4\lambda$, $L_{pd} = 1\lambda$, $W_{pd} = 8\lambda$
 Inverter-B
 $L_{pu} = 4\lambda$, $W_{pu} = 4\lambda$, $L_{pd} = 2\lambda$, $W_{pd} = 8\lambda$



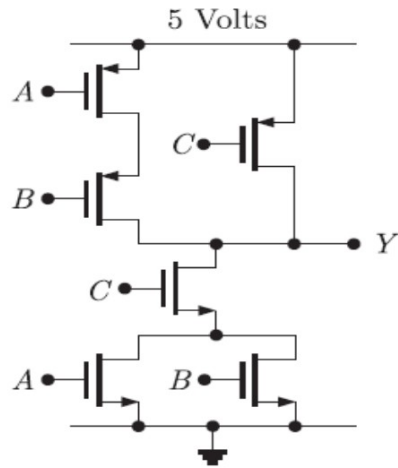
56. (a) Design a magnitude comparator based on the data path operators.
 (b) Draw the Schematic and mask layout of array adder used in Booth Multiplier and explain the principle of multiplication in Booth Multiplier.
57. Write briefly about:
 (a) Channeled gate arrays
 (b) Channel less gate arrays with neat sketches.
58. (a) Draw the basic structure of parallel scan and explain how it reduces the long scan chains.
 (b) Draw the state diagram of TAP Controller and explain how it provides the control signals for test data and instruction register.
59. (a) What is the principle of FPGAs? Explain about the architectures of FPGAs.
 (b) What are the applications of FPGAs? Explain.
60. Draw the circuit for NMOS Inverter and explain its operation.
61. (a) Explain the processing steps in fabrication of nmos technology with neat sketches.
 (b) Explain any one method of encapsulation of IC.
62. Write notes on any TWO
 (a) DGT
 (b) BIST
 (c) Boundary scan Testing.
63. Give the topology for four bit carry select module and explain its operation in detail.

64. (a) Design a complimentary static CMOS XOR gate. Explain the steps involved and draw the logic circuit.
 (b) What are the issues involved in driving large capacitor loads in VLSI circuit designs? Explain.
65. (a) Explain about the effect of scaling on MOSFET parameters.
 i. Gate Area
 ii. Gate capacitance
 iii. Channel Resistance
 iv. Transistor Delay
 (b) Explain about Design Rules for contact cuts.
66. (a) Draw the circuit and layout schematic for 2-input NOR gate giving explanation.
 (b) What are the various limitations of scaling?
67. Draw the circuit for CMOS inverter and explain the transfer characteristic using necessary equations, and the different regions in the characteristic.
68. (a) Give a schematic for memory self-test and explain the same.
 (b) What are the advantages of implementing BIST? Explain.
69. What are the circuit design considerations in the case of static adder circuits?
70. (a) With the help of sketches explain the principles of different types of diffusion Processes.
 (b) Explain about Fick's laws of diffusion.
71. (a) Explain the structure and principle of PLA.
 (b) Draw the schematic and explain how Full Adder can be implemented using PLA's.
72. (a) Explain the concept of sheet resistance and sheet capacitance. Give examples.
 (b) What are the design issues involved in long interconnect wires? Explain.
73. (a) Explain the processing steps in fabrication of PMOS technology with neat sketches.
 (b) What are the additional two layers in BICMOS technology compared to others?
74. (a) Explain about stick diagram.
 (b) Explain about scaling.
75. (a) Draw the circuit of CMOS Inverter and explain its operation.
 (b) What are the various pull up transistor used for inverters?
76. (a) What are the issues involved in driving large capacitive loads in VLSI circuits? Explain.
 (b) Derive the expression for τ_{SD} in the case of a MOSFET.
77. (a) With the help of a schematic explain about Memory-self Test.
 (b) What are the issues to be considered while implementing BIST? Explain.

78. Draw the schematic for Wallace Tree for four bit Multiplier and explain its operation.
79. (a) Draw the structure of programmable Array logic(PAL) and explain its principle of operation.
(b) Explain about different methods of implementation approaches in VLSI Design.
80. Explain the principle and working of CPLDs and give their applications.
81. (a) With the help of flow chart explain the method of Testing at various stages in VLSI Design cycle.
(b) Why testing is needed in VLSI design? Explain the principle of testing.
82. Draw the circuits for n-MOS, p-MOS and C-MOS Inverter and explain about their operation and compare them.
83. (a) Explain about bit sliced Data path organization. What is the significance of Data paths in digital processors?
(b) Give the Truth Table for full adder and explain its Boolean expression.
84. (a) What are the different types of oxidation processes? Explain.
(b) With the help of neat sketches, explain the steps involved in photolithography and pattern transfer.
85. Explain about Static Logic, Dynamic Logic and Domino Logic and compare them in all respects.
86. (a) Why scaling is required?
(b) How does Depletion Regions around Source and Drain are affected due to scaling down of device dimensions? Explain.

(10.2) QUESTION BANK – GATE

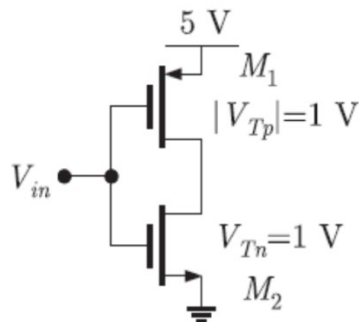
1. In the circuit shown
GATE 2012



- (A) $Y = \overline{A} \overline{B} + \overline{C}$ (B) $Y = (A + B) C$
 (C) $Y = (\overline{A} + \overline{B}) \overline{C}$ (D) $Y = AB + C$

2. In the CMOS circuit shown, electron and hole mobilities are equal, and M_1 and M_2 are equally sized. The device M_1 is in the linear region if

GA
TE
2012

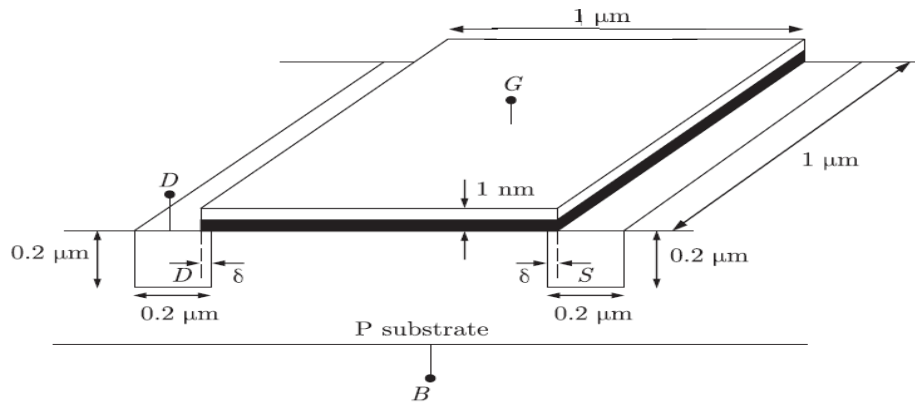


- (A) $V_{in} < 1.875 \text{ V}$ (B) $1.875 \text{ V} < V_{in} < 3.125 \text{ V}$
 (C) $V_{in} > 3.125 \text{ V}$ (D) $0 < V_{in} < 5 \text{ V}$

Common Data for Question 3 and 4 :

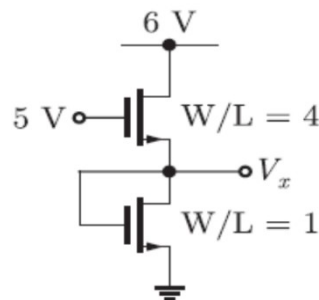
GATE 2012

In the three dimensional view of a silicon n -channel MOS transistor shown below, $\delta = 20 \text{ nm}$. The transistor is of width $1 \mu\text{m}$. The depletion width formed at every p - n junction is 10 nm . The relative permittivity of Si and SiO₂, respectively, are 11.7 and 3.9, and $\epsilon_0 = 8.9 \times 10^{-14} \text{ F/m}$



3. The gate source overlap capacitance is approximately
 (A) 0.7 fF (B) 0.7 pF
 (C) 0.35 fF (D) 0.24 pF
4. The source-body junction capacitance is approximately
 (A) 2 fF (B) 7 fF
 (C) 2 pF (D) 7 pF
5. In the circuit shown below, for the MOS transistors, $\mu_n C_{ox} = 100 \text{ A/V}^2$ and the threshold voltage $V_T = 1 \text{ V}$. The voltage V_x at the source of the upper transistor is

GATE 2011

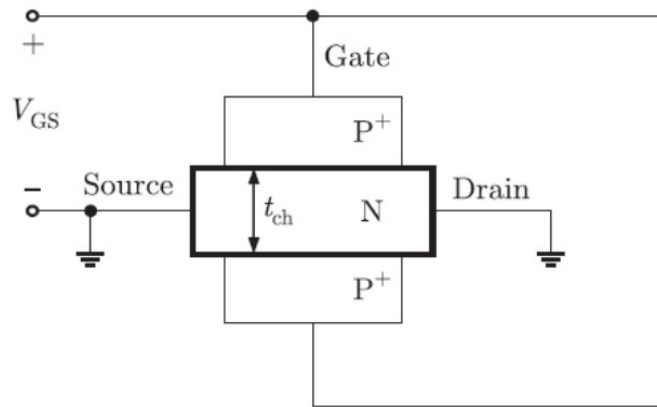


- (A) 1 V (B) 2 V
 (C) 3 V (D) 3.67 V

Common Data Questions: 6 & 7

GATE 2011

The channel resistance of an N-channel JFET shown in the figure below is 600Ω when the full channel thickness (t_{ch}) of $10 \mu\text{m}$ is available for conduction. The built in voltage of the gate P^+N junction (V_{bi}) is -1 V . When the gate to source voltage (V_{GS}) is 0 V , the channel is depleted by $1 \mu\text{m}$ on each side due to the built in voltage and hence the thickness available for conduction is only $8 \mu\text{m}$



6. The channel resistance when $V_{GS} = -3 \text{ V}$ is
 (A) 360Ω (B) 917Ω
 (C) 1000Ω (D) 3000Ω
7. The channel resistance when $V_{GS} = 0 \text{ V}$ is
 (A) 480Ω (B) 600Ω
 (C) 750Ω (D) 1000Ω
8. At room temperature, a possible value for the mobility of electrons in the inversion layer of a silicon n -channel MOSFET is
 GATE 2010
 (A) $450 \text{ cm}^2/\text{V-s}$ (B) $1350 \text{ cm}^2/\text{V-s}$
 (C) $1800 \text{ cm}^2/\text{V-s}$ (D) $3600 \text{ cm}^2/\text{V-s}$
9. Thin gate oxide in a CMOS process is preferably grown using
 GATE 2010
 (A) wet oxidation (B) dry oxidation
 (C) epitaxial oxidation (D) ion implantation

(10.3) QUESTION BANK – IES

1. A gate to drain-connected enhancement mode MOSFET is an example of
 IES 2012
 (a) an active load (b) a switching device
 (c) a three-terminal device (d) a three-terminal device
2. Body effect in MOSFETs results in
 IES 2012
 (a) increase in the value of transconductance
 (b) change in the value of threshold voltage
 (c) decrease in the value of transconductance
 (d) increase in the value of output resistance
3. Assertion (A) : Si mainly used for making ICs and not Ge.
 IES 2011

Reason(R) : In Si, SiO₂ layer which acts as an insulator can be formed for isolation purposes. Corresponding oxide layer cannot be formed in Ge.

(11) Two case study presentations with Project / Product/ Model /prototypes/ Industrial applications:

1. Design Wallace Tree Multiplier Using Reversible Gates

Multipliers are essential components in digital circuit design. They have wide spread applications in digital signal processing and communication systems. Circuit designers in VLSI design seek compact, small scale circuits with low power consumption and minimal delay. The Wallace tree multiplier is an advanced version of tree based multipliers. Numerous algorithms have been developed to create the fastest multipliers, and the Wallace tree multiplier is one such example. It utilizes reversible compressors, full adders, and half adders. The results demonstrate that the Wallace tree multiplier using reversible gates outperforms traditional multipliers in terms of power dissipation and delay, with values of 0.027W and 29.327nS respectively.

Link:- <https://www.ijraset.com/research-paper/design-wallace-tree-multiplier-using-reversible-gates>

2. A novel design of 1-bit full adders for eliminating voltage step in BBL-PT full adder using 32-nm CNTFET technology

The full adder is essential for building computing systems like multipliers. Optimizing its design with CNTFET technology enhances low power, speed, and circuit density. This article presents a novel approach to address the challenges in Branch-Based Logic and Pass-Transistor (BBL-PT) based 1-bit full adder. The proposed approach involves the use of alternative modified level restorers, including a current sink, D-CNTFET (Diode connected CNTFET), modified current sink, and source structures. The BBL-PT full adder suffers from a voltage step issue in its output. The proposed solution eliminates this drawback using four alternative restorer structures. For +0.9 V supply voltage at 32-nm CNTFET technology, among all the proposed adder designs, the current sink based adder has a reported power consumption of 0.0845 μ W, which is exceptionally low with the propagation delay is specified as 6.127 Ps and the Power-Delay Product (PDP) is 0.5177 aJ. The deliberate use of the current sink restorer in the design contributes to achieving these exceptional performance characteristics. An N-bit parallel adder (N=8, 16 & 32) using the proposed full adders is presented, with performance evaluated at 32-nm CNTFET technology and +0.9 V supply using Mentor Graphics tools. Results highlight its efficiency and superiority over existing solutions.

Link:- <https://www.tandfonline.com/doi/full/10.1080/00207217.2025.2450735>

(12) Assignment Question sets:

Unit – I

SET 1:

1. With neat sketches explain the electron lithography process.
2. Derive the relationship between drain current I_d versus drain to source voltage V_{ds} in active region and saturation region.
3. What are different forms of Pull – ups? Determine the Pull-up to Pull – down of an NMOS Inverter driven by another NMOS Transistor.
4. Explain the advantages of MOS technology over the bipolar technology and why MOS devices gained predominance over bipolar devices?

SET 2:

1. Explain the operation of BiCMOS inverter? Clearly specify its characteristics.
2. Explain the various steps in PMOS Fabrication.
3. Explain the process flow of CMOS Fabrication.
4. Compare NMOS & CMOS Technologies.

SET 3:

1. Describe the two commonly used methods for obtaining integrated capacitor.
2. With neat sketches, explain in detail, all the steps involved in electron lithography process.
3. What is Moore's law? Explain its relevance with respect to evolution of IC Technology.
4. What is the size of silicon wafer used for manufacturing state-of-the art VLSI ICs?

SET 4:

1. What is the minimum feature size of current commercial VLSI devices?
2. Explain the following:
 - (a) Thermal oxidation technique
 - (b) Kinetics of thermal oxidation.
3. With neat sketches explain how NPN transistor is fabricated in bipolar process.
4. With neat sketches explain how Diodes and Resistors are fabricated in NMOS Process.

Unit – II

SET 1:

1. Size the devices and draw the stick diagram of a CMOS, and NMOS inverter circuits.

2. Do the NMOS and CMOS implementations of the circuit for function whose logic is given by Also draw it's layout:

$$Y = (A+B).C$$

3. Derive the propagation delay of a depletion mode n-channel MOSFET.
4. Derive the pull-down ratio of a CMOS inverter.

SET 2:

1. Derive the pull-up to pull-down ratio of a CMOS inverter.
2. What is a stick diagram? Draw the stick diagram and layout for a CMOS Inverter.
3. What are the effects of scaling on V_t ?
4. What are design rules? Why is metal- metal spacing larger than poly –poly spacing.

SET 3:

1. Draw the stick diagram and mask layout for a CMOS two input NOR gate and Stick diagram of two input NAND gate.
2. Draw the stick diagram and a translated mask layout for nMOS inverter circuit.
3. Explain the following
 - (a) Double metal MOS process rules.
 - (b) Design rules for P- well CMOS process
4. Design a stick diagram for two input n-MOS NAND and NOR gates.

SET 4:

1. Design a stick diagram for the NMOS logic shown below $Y = (A + B + C)'$.
2. Design a stick diagram for n-MOS Ex-NOR gate.
3. Design a stick diagram for the PMOS logic shown below $Y = ((A + B).C)'$.
4. Design a layout diagram for the PMOS logic shown below $Y = (AB)' + (CD)'$.

Unit - III

SET 1:

1. Implement the logic diagram for the Boolean equation $Y = (A+B).(C+D)$ after sizing the transistors. Do the NMOS and CMOS implementations.

2. Do the NMOS and CMOS implementations of the circuit for the function whose logic is given by $Y = (A+B).C$
3. Explain how the resistance of a non-rectangular region can be measured?
4. Calculate the rise time and fall time of the CMOS inverter $(W/L)_n = 6$ and $(W/L)_p = 8$, $K'_n = 150 \mu A/V^2$, $V_{tn} = 0.7V$, $K'_p = 62 \mu A/V^2$, $V_{tp} = -0.85V$, $V_{DD} = 3.3V$. Total out-put capacitance $= 150$ fF.

SET 2:

1. Explain the concept of sheet resistance and apply it to compute the ON resistance (V_{DD} to GND) of an NMOS inverter having pull up to pull down ratio of 4:1, If n channel resistance is $R_{sn} = 10^4$ per square.
2. Calculate the gate capacitance value of $5\mu m$ technology minimum size transistor with gate to channel capacitance value is $4 \times 10^{-4} pF/\mu m^2$.
3. Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit.
4. Define and explain the following:
 - i. Sheet resistance concept applied to MOS transistors and inverters.
 - ii. Standard unit of capacitance.

SET 3:

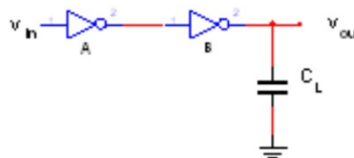
1. Explain the requirement and functioning of a delay unit.
2. Two nMOS inverters are cascaded to drive a capacitive load $C_L = 14C_g$ as shown in Figure. Calculate the pair delay V_{in} to V_{out} in terms of τ for the given data.

Inverter -A

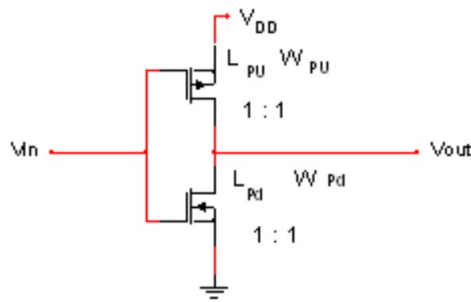
$LP.U = 12\lambda$, $WP.U = 4\lambda$, $LP.d = 1\lambda$, $WP.d = 1\lambda$

Inverter -B

$LP.U = 4\lambda$, $WP.U = 4\lambda$, $LP.d = 2\lambda$, $WP.d = 8\lambda$



3. Calculate on resistance of the circuit shown in Figure 1 from V_{DD} to GND. If n-Channel sheet resistance $R_{sn} = 10^4$ per square and p-channel sheet resistance $R_{sp} = 2.5 \times 10^4$ per square.



4. Calculate the gate capacitance value of $2\mu\text{m}$ technology minimum size transistor with gate to channel capacitance value is $8 \times 10^{-4} \text{pF}/\mu\text{m}^2$.

SET 4:

1. Explain clearly about different parasitic capacitances of an nMOS transistor.
2. Do the NMOS and CMOS implementations of the circuit for the function whose logic is given by $Y = (A+B).C$
3. Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit.
4. Explain how the resistance of a non-rectangular region can be measured?

Unit - IV

SET 1:

1. Design a logic gate network for the full adder using two-level logic; using multi-level logic.
2. What is the false delay path in the carry-skip adder?
3. Design the logic for an ALU that can perform these functions: addition, subtraction, AND, OR, NOT.
4. Design components of a Booth multiplier.

SET 2:

1. Design the logic for one bit of the adder-subtractor.
2. Design a stick diagram for adder-subtractor.
3. Design and analyze an 8×8 Wallace tree multiplier.
4. Draw the block diagram for an eight-bit carry save adder.

SET 3:

1. Draw the complete block diagram for the 8 x 8 Wallace tree multiplier.
2. What is the minimum-delay encoding for a modulo-8 counter?
3. Explain the CMOS system design based on the data path operators with asuitable example.
4. Draw and explain the basic Memory- chip architecture.

SET 4:

1. Explain the CMOS system design based on the data path operators with asuitable example.
2. Draw and explain the basic Memory- chip architecture.
3. Compare the different types of CMOS subsystem Multipliers.
4. Design a schematic for an 8-word \times 2-bit NAND ROM that serves a lookuptable to implement a full adder.

Unit –V

SET 1:

1. What are the advantages and disadvantages of ASIC design approach?
2. Give the block diagram of PLA device and explain about the PLA.
3. Draw the basic structure of parallel scan and explain how it reduces the long scan chains.
4. Explain how ROM can be used as PLD.

SET 2:

1. Explain about the three different approaches for the formation of logic cell using FPGA implementation.
2. Explain the function of 4:1 Mux in PAL CMOS device with the help of I/O structure.
3. Explain how the pass transistors are used to connect wire segments for the purpose of FPGA programming.
4. Explain the methods of programming of PAL CMOS device.

SET 3:

1. Draw and explain the architecture of an FPGA.
1. Draw the basic structure of parallel scan and explain how it reduces the long scan chains.
2. Explain any one chip architecture that used the antifuse and give its advantages.

3. Draw the typical standard-cell structure showing low-power cell and explain it.

SET 4:

1. Sketch a diagram for two input XOR using PLA and explain its operation with the help of truth table.
2. Using PLA Implement JK Flip flop circuit.
3. With neat sketches explain the architecture of PAL.
4. Explain about the different test techniques such as scan based, self test and IDDQ testing.

(13) List of topics for students Seminars

1. Static Timing Analysis
2. Analog Memories
3. Nano-RAM
4. Organic LED
5. M-RAM(Magneto Resistance Random Access Memory)
6. Multi Threshold CMOS
7. Low Leak Transistor
8. MESFET
9. Single Electron Tunneling Technology
10. Extreme Ultra Violet Lithography
11. MEMS (Micro Electro Mechanical Systems)
12. Photonic Integration of Hybrid Silicon

(14) STEP/Course material in softcopy

1. How do you prevent latch up problem?

Latch up problem can be reduced by reducing the gain of parasitic transistors and resistors. It can be prevented in 2 ways

•Latch up resistant CMOS program •Layout technique

The various lay out techniques are

Internal latch up prevention technique

I/O latch up prevention technique.

2. List the basic process for IC fabrication

Silicon wafer Preparation _ Epitaxial Growth

Oxidation

Photolithography _ Diffusion

Ion Implantation _ Isolation technique _ Metallization

Assembly processing & Packaging

3. What are the various Silicon wafer Preparation?

Crystal growth & doping

Ingots trimming & grinding _ Ingot slicing

Wafer polishing & etching _ Wafer cleaning.

4. Different types of oxidation?

Dry & Wet Oxidation

5. What are the advantages of CMOS process?

Low power Dissipation High Packing density Bi directional capability Low Input Impedance
Low delay Sensitivity to load.

6. What is pull down device?

A device connected so as to pull the output voltage to the lower supply voltage usually 0V is called pull down device.

7. What is pull up device?

A device connected so as to pull the output voltage to the upper supply voltage usually VDD is called pull up device.

8.. Why NMOS technology is preferred more than PMOS technology?

N- channel transistors has greater switching speed when compared to PMOS transistors.

9. What are the different operating regions for an MOS transistor?

_ Cutoff region

_ Non- Saturated Region _ Saturated Region

10. What is Channel-length modulation?

The current between drain and source terminals is constant and independent of the applied voltage over the terminals. This is not entirely correct. The effective length of the conductive channel is actually modulated by the applied VDS, increasing VDS causes the depletion region at the drain junction to grow, reducing the length of the effective channel.

11. What is Latch – up?

Latch up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between VDD and VSS with disastrous results. Careful control during fabrication is necessary to avoid this problem.

UNIT-2

1. What is Stick Diagram?

It is used to convey information through the use of color code. Also it is the cartoon of a chip layout.

2. What are the uses of Stick diagram?

It can be drawn much easier and faster than a complex layout.

These are especially important tools for layout built from large cells.

3. Give the various color coding used in stick diagram?

- _ Green –n-diffusion _ Red- polysilicon
- _ Blue –metal
- _ Yellow- implant
- _ Black-contact areas.

4. Define Threshold voltage in CMOS?

The Threshold voltage, V_T for a MOS transistor can be defined as the voltage applied between the gate and the source of the MOS transistor below which the drain to source current, I_{DS} effectively drops to zero.

5. What is Body effect?

The threshold voltage V_T is not a constant w. r. to the voltage difference between the substrate and the source of MOS transistor. This effect is called substrate-bias effect or body effect.

6. What are the various CMOS technologies?

Various cmos technologies are,

- i) n- well process or n -tub process
- ii) p well process or p-tub process
- iii) Twin tub process
- iv) Silicon on Insulator (SOI) process

7. What is channel-stop implantation?

In n -well fabrication, n-well is protected with resist material. Because it should not be affected by boron implantation. Then boron is implanted except n-well. It is done using photo resist mask. This type of implantation is known as channel-stop implantation.

8. What is LOCOS?

LOCOS mean Local Oxidation of Silicon. This is one type of oxide construction.

9. What is LDD?

LDD means Lightly Doped Drain structures. It is used for implantation of n-in n-well process.

10. What is twin tub process? Why it is so called?

Twin tub process is one of cmos technology. There are two wells available in this process.

The other name of well is tub. so because of these two tubs, this process is known as twin tub process.

11. What are the special features of twin tub process?

In twin tub process, threshold voltages, body effect of n and p devices are independently optimized.

12. What are the advantages of twin tub process?

Advantages of twin tub process are

- 1) Separate optimized wells are available.
- 2) Balanced performance is obtained for n and p transistors.

16. What is meant by interconnect? What are the types of interconnect?

Interconnect means connection between various components in an IC Types of Interconnect
Metal Interconnect

Polysilicon Inter connect.

Local Inter Connect.

17. What are the two types of Layout design rules?

Lambda (λ) design rules and micron rules are major types of layout design rules.

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N- channel transistors has greater switching speed when compared to PMOS transistors.

21. What are the different operating regions for an MOS transistor?

_ Cutoff region

_ Non- Saturated Region _ Saturated Region

22. What are the different MOS layers?

N- Diffusion

P- Diffusion

SIO₂

UNIT 3

1. Which MOS can pass logic 1 and logic 0 strongly?

p-mos can pass strong logic 1 n-mos can pass strong logic 0.

2. What is meant by a transmission gate?

A transmission gate consists of an n-channel transistor and p-channel transistor with separate gates and common source and drain. Its symbol is

3. Write the design style classification?

The IC design style can be classified as

(1) Full custom Design ASICs

(2) Semi custom Design ASICs

(a) Standard Cell Design

(b) Gate Array Design

(i) Channeled Gate Array

(ii) Channel less Gate Array

(3) Programmable ASICs

(a) PLDs

(b) FPGA

4. What are the two types of ASICs ?

Types of ASICs are

Full custom ASICs

Semi custom ASICs

5. What are the types of programmable devices?

Types of programmable devices are

(1) Programmable Logic Structure

- (2)Programmable Interconnect.
- (3)Reprogrammable Gate Array.

6. What are the different types of programming structure available in PAL?

Programming Techniques of PAL are

- (1)Fusible links programming
- (2)UV-Erasable EPROM programming
- (3)EEPROM programming

7. Why CMOS technology is most useful for analog functions?

The first reason is that CMOS is now by far the most widely available IC technology. Most CMOS Asics and CMOS standard products are now being manufactured than bipolar ICs. The second reason is that increased levels of integration require mixing analog and digital functions on the same IC: this has forced designers to find ways to use CMOS technology to implement analog functions.

UNIT-4

1. What are the features of standard celled ASICs?

All mask layers are customized- transistors and interconnect.

Custom blocks can be embedded.

Manufacturing lead time is about eight weeks.

2. What is the difference between channeled gate array and channel less gate array?

The key difference between a channel less gate array and channeled gate array is that there are no predefined areas set aside for routing between cells on a channel less gate array.

Instead we route over the top of the gate –array devices. We can do this because we customize the contact defines the connections between metall, the first layer of metal and the transistors.

3. What are the characteristics of FPGA?

None of the mask layers are customized

- A method for programming the basic logic cells and the interconnect.
 - The core is a regular array of programmable basic logic cells that can implement combinational as well as sequential logic (flip-flops).
- A matrix of programmable interconnect surrounds the basic logic cells.
- Design turnaround is a few hours.

4. What is programmable logic array?

A programmable logic array (PLA) is a programmable device used to implement combinational logic circuits. The PLA has a set of programmable AND planes, which link to a set of programmable OR planes, which can then be conditionally complemented to produce an output an output. This layout allows for a large number of logic functions to be synthesized in the sum of products (and sometimes product of sums) canonical forms.

6. What is mean by Programmable logic plane?

The Programmable logic plane is programmable read-only memory (PROM) array that allows the signals present on the devices pins (or the logical components of those signals) to be routed to an output logic macro cell.

7. Describe the steps in ASIC design flow?

- Design entry. Enter the design into an ASIC design system, either using a hardware description language (HDL) or schematic entry.
- Logic synthesis. Use an HDL (VHDL or Verilog) and a logic synthesis tool to produce a net list
 - a description of the logic cells and their connections.
- System partitioning. Divide a large system into ASIC- sized pieces.
- Prelayout simulation. Check to see if the design functions correctly.
- Floor planning. Arrange the blocks of the net list on the chip.
- Placement. Decide the locations of cells in a block.
- Routing. Make the connections between cells and blocks.
- Extraction. Determine the resistance and capacitance of the interconnect.
- Post layout simulation. Check to see the design still works with the added loads of the inter connect.

8. Give the application of PLA

Design and testing of digital circuits

17. What is the full custom ASIC design?

In a full custom ASIC, an engineer designs some or all of the logic cells, circuits or layout specifically for one ASIC. It makes sense to take this approach only if there are no suitable existing cell libraries available that can be used for the entire design.

9. What is the standard cell-based ASIC design?

A cell-based ASIC (CBIC) uses predesigned logic cells known as standard cells. The standard cell areas also called flexible blocks in a CBIC are built of rows of standard cells. The ASIC designer defines only the placement of standard cells and the interconnect in a CBIC. All the mask layers of a CBIC are customized and are unique to a particular customer.

10. Give the constituent of I/O cell in 22V10.

2V10 I/O cell consists of

- 1.a register
- 2.an output 4:1 mux
- 3.a tristate buffer
- 4.a 2:1 input mux

It has the following characteristics:

- *12 inputs
- *10 I/Os
- *product time 9 10 12 14 16 14 12 10 8
- *24 pins

11. What is a FPGA?

A field programmable gate array (FPGA) is a programmable logic device that supports implementation of relatively large logic circuits. FPGAs can be used to implement a logic circuit with more than 20,000 gates whereas a CPLD can implement circuits of upto about 20,000 equivalent gates.

12. What are the different methods of programming of PALs?

The programming of PALs is done in three main ways: Fusible links

UV – erasable EPROM

EEPROM (E 2PROM) – Electrically Erasable Programmable ROM.

14. What are the different levels of design abstraction at physical design?

Architectural or functional level

Register Transfer-level (RTL) Logic level

Circuit level

15. What are macros?

The logic cells in a gate-array library are often called macros.

16. What are Programmable Interconnects?

In a PAL, the device is programmed by changing the characteristics of the switching element.

An alternative would be to program the routing.

17. What are the types of gate arrays in ASIC?

1) Channel gate arrays

2) Channel less gate arrays

3) Structured gate arrays

18. Mention the common techniques involved in ad hoc testing?

Partitioning large sequential circuits

Adding test points

Adding multiplexers

providing for easy state reset

19. What are the scan-based test techniques?

a) Level sensitive scan design

b) Serial scan

c) Partial serial scan

d) Parallel scan

20. What are the two tenets in LSSD?

a. The circuit is level-sensitive.

b. Each register may be converted to a serial shift register.

21. What are the self-test techniques?

a. Signature analysis and BILBO

b. Memory self-test

c. Iterative logic array testing

22. What is known as BILBO?

Signature analysis can be merged with the scan technique to create a structure known as BILBO- for Built In Logic Block Observation.

23. What is known as IDDQ testing?

A popular method of testing for bridging faults is called IDDQ or current supply monitoring.

This relies on the fact that when a complementary CMOS.

Logic gate is not switching, it draws no DC current. When a bridging fault occurs, for some combination of input conditions a measurable DC IDD will flow.

24. What are the applications of chip level test techniques?

a. Regular logic arrays

b. Memories

c. Random logic

26. What is boundary scan?

The increasing complexity of boards and the movement to technologies like multichip modules and surface-mount technologies resulted in system designers agreeing on a unified scan-based methodology for testing chips at the board. This is called boundary scan.

27. What is the test access port?

The Test Access Port (TAP) is a definition of the interface that needs to be included in an IC to make it capable of being included in a boundary-scan architecture. The port has four or five single bit connections, as follows:

TCK (The Test Clock Input)

TMS (The Test Mode Select) TDI(The Test Data Input) TDO(The Test Data Output)

It also has an optional signal TRST*(The Test Reset Signal).

28. What are the contents of the test architecture?

The test architecture consists of:

The TAP interface pins A set of test-data registers An instruction register

A TAP controller

29. What is the TAP controller?

The TAP controller is a 16-state FSM that proceeds from state to state based on the TCK and TMS signals. It provides signals that control the test data registers, and the instruction register. These include serial-shift clocks and update clocks.

30. What is known as test data register?

The test-data registers are used to set the inputs of modules to be tested, and to collect the results of running tests.

31. What is known as boundary scan register?

The boundary scan register is a special case of a data register. It allows circuit-board interconnections to be tested, external components tested, and the state of chip digital I/Os to be sampled.

32. Mention the levels at which testing of a chip can be done?

- a) At the wafer level
- b) At the packaged-chip level
- c) At the board level
- d) At the system level
- e) In the field

33. Expert Lectures with topics & Schedules (if any)

Stick diagrams and Layouts on the month of February.

Emerging Issues in VLSI Design on the month of March.

UNIT 5**1. What are the different types of CMOS testing**

Functionality tests manufacturing tests

2. What is the aim of adhoc test techniques?

The adhoc test techniques are aimed at reducing the combinational explosion of testing.

3. Distinguish functionality test and manufacturing test

Functionality tests seek to verify that a chip as a whole is functionally equivalent to some specification, whereas manufacturing tests are used to verify that every gate operates as expected.

4. List any two faults that occur during manufacturing

1. Stuck at fault
 - (a) Stuck at 0 fault
 - (b) Stuck at 1 fault
2. SC & OC faults
 - (a) Short circuit model fault
 - (b) Open circuit model fault

5. What is the need for testing?

IC fabrication is a very complex process. So, there may be any imperfection occur in any one of the stage. This imperfection may affect the result. So testing is necessary to find out which IC is good and which IC is bad.

6. Write notes on functionality tests?

Functionality tests verify that the chip performs its intended function. These tests assert that all the gates in the chip, acting in concert, achieve a desired function. These tests are usually used early in the design cycle to verify the functionality of the circuit.

7. Write notes on manufacturing tests?

Manufacturing tests verify that every gate and register in the chip functions correctly. These tests are used after the chip is manufactured to verify that the silicon is intact.

8. Mention the defects that occur in a chip?

- a) layer-to-layer shorts
- b) discontinuous wires
- c) thin-oxide shorts to substrate or well

9. Give some circuit maladies to overcome the defects?

- i. nodes shorted to power or ground
- ii. nodes shorted to each other
- iii. inputs floating/outputs disconnected

10. What are the tests for I/O integrity?

- i. I/O level test
- ii. Speed test
- iii. IDD test

11. What is meant by fault models?

Fault model is a model for how faults occur and their impact on circuits.

12. Give some examples of fault models?

- i. Stuck-At Faults
- ii. Short-Circuit and Open-Circuit Faults

13. What is stuck – at fault?

With this model, a faulty gate input is modeled as a “stuck at zero” or “stuck at one”. These faults most frequently occur due to thin-oxide shorts or metal-to-metal shorts.

14. What is meant by observability?

The observability of a particular internal circuit node is the degree to which one can observe that node at the outputs of an integrated circuit.

15. What is meant by controllability?

The controllability of an internal circuit node within a chip is a measure of the ease of setting the node to a 1 or 0 state.

16. What is known as percentage-fault coverage?

The total number of nodes that, when set to 1 or 0, do result in the detection of the fault, divided by the total number of nodes in the circuit, is called the percentage-fault coverage.

17. What is fault grading?

Fault grading consists of two steps. First, the node to be faulted is selected. A simulation is run with no faults inserted, and the results of this simulation are saved. Each node or line to be faulted is set to 0 and then 1 and the test vector set is applied. If and when a discrepancy is detected between the faulted circuit response and the good circuit response, the fault is said to be detected and the simulation is stopped.

18. Mention the ideas to increase the speed of fault simulation?

- a. Parallel simulation
- b. Concurrent simulation

19. What is fault sampling?

An approach to fault analysis is known as fault sampling. This is used in circuits where it is impossible to fault every node in the circuit. Nodes are randomly selected and faulted. The resulting fault detection rate may be statistically inferred from the number of faults that are detected in the fault set and the size of the set. The randomly selected faults are unbiased. It will determine whether the fault coverage exceeds a desired level.

20. What are the approaches in design for testability?

- a. ad hoc testing
- b. scan-based approaches
- c. self-test and built-in testing

21. Mention the common techniques involved in ad hoc testing?

- d. partitioning large sequential circuits
- e. adding test points
- f. adding multiplexers
- g. providing for easy state reset

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S.NO	SUBJECT	TOPIC	YEAR	RESOURCE PERSON	DATE
1	VLSID	Emerging Issues in VLSI Design	III-II	Others	March,2025